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Structurally Engineered Nanoporous Ta_2O_{5-x} Selector-Less Memristor for High Uniformity and Low Power Consumption

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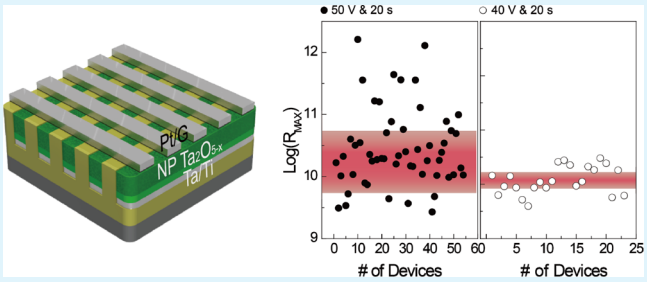
Supporting Information

ABSTRACT: A memristor architecture based on metal-oxide materials would have great promise in achieving exceptional energy efficiency and higher scalability in next-generation electronic memory systems. Here, we propose a facile method for fabricating selector-less memristor arrays using an engineered nanoporous Ta_2O_{5-x} architecture. The device was fabricated in the form of crossbar arrays, and it functions as a switchable rectifier with a self-embedded nonlinear switching behavior and ultralow power consumption (~2.7 × 10^{-6} W), which results in effective suppression of crosstalk interference. In addition, we determined that the essential switching elements, such as the programming power, the sneak current, the nonlinearity value, and the device-to-device uniformity, could be enhanced by in-depth structural engineering of the pores in the Ta_2O_{5-x} layer. Our results, on the basis of the structural engineering of metal-oxide materials, could provide an attractive approach for fabricating simple and cost-efficient memristor arrays with acceptable device uniformity and low power consumption without the need for additional addressing selectors.



KEYWORDS: *memristor, metal-oxide, tantalum oxide, nonlinear switching, ultralow power consumption*

INTRODUCTION

Memristive devices with a simple metal-oxide layer sandwiched between two conducting electrodes have been put forward as promising candidates to meet the high standards required for "next-generation universal memories," such as nanoscale device footprints, fast operation, low fabrication cost, and exceptional power efficiency.[1−5] A crossbar array architecture in which an active memristor is formed at every cross-point has become a platform technology because the structure provides a high density and a simple method for integrating resistive random-access memory (ReRAM).[6−10] Despite the geometrical and conceptual simplicity of the crossbar array structure, the future of high-density memristor arrays depends on breakthroughs in both material development for two basic components (the selector and the storage element at a node) and an integrated architecture for the crossbar array configuration.[2−4,6−9]

In an operational array structure, an individual selector such as a transistor, diode, or threshold switching device must be integrated with each storage element to reliably access its innate switching state.[6−9,11−13] However, these additional selector components could constrain the scaling limits of ReRAMs[6,14−16] and create complexity in the crossbar array fabrication procedure that may diminish the fabrication yield and the switching uniformity of the devices.[2−4,6−13] In this sense, a device concept exhibiting a self-embedded nonlinear switching behavior, referred to as a selector-less memristor, has been highlighted as a potential approach for next-generation memory.[4,9,10,15]

Recently, we fabricated a single device from a nanoporous (NP) Ta_2O_5-based memristor and proposed its potential for use as a selector-less memristor because it showed a highly nonlinear self-rectifying $I-V$ switching behavior.[15] However, despite this feature, the inhomogeneous diameter of the pores could not only significantly impact the device-to-device uniformity, causing a large variation of essential switching elements and programming paths but could also restrict the optimal switching functionalities, as well as the scalability of a memristor array. In addition, it is also important to investigate

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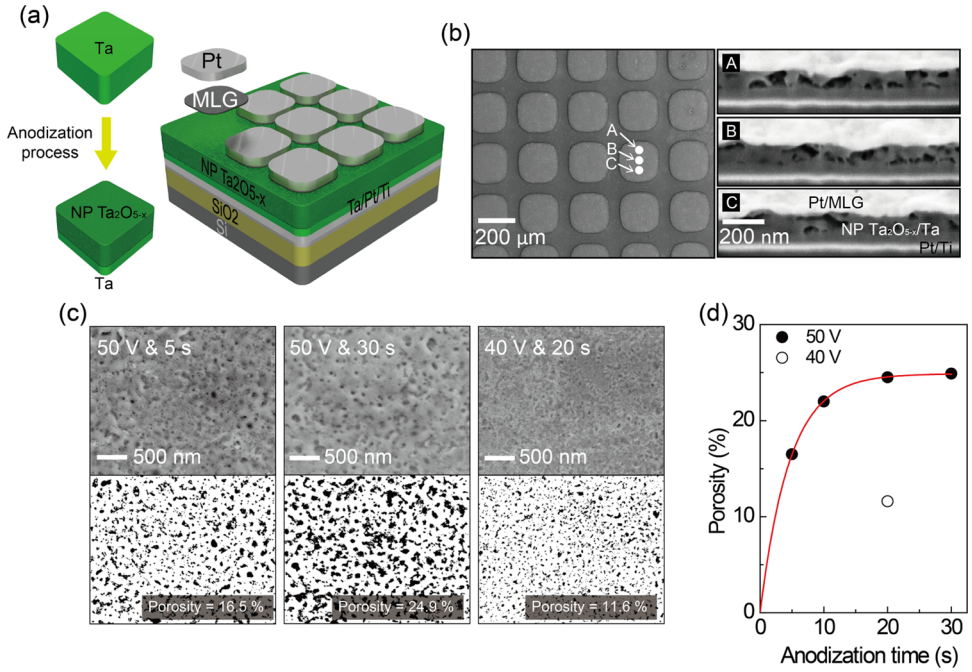

Figure 1. (a) Schematic illustrations of the cells in the NP Ta_2O_{5-x} memristor device and the electrochemical anodization process of the Ta metal. (b) Top-view SEM image of the NP Ta_2O_{5-x} memristor device (left); the side length of the cell is 200 μm. Cross-sectional SEM images of the NP Ta_2O_{5-x} memristor device showing three different locations (A−C) of the cell (right). Note that the anodization was performed at 50 V for 20 s. (c) Top-view SEM images of the NP Ta_2O_{5-x} film and the corresponding high-contrast images for different anodization conditions. The black and white regions in the high-contrast images represent the pores and the Ta_2O_{5-x} film region, respectively. (d) Estimated porosity for different anodization conditions; the measurements were obtained at specific dc voltages (40 and 50 V) and for different anodization times (5, 10, 20, and 30 s).

the relationship between the switching elements and the different pore structures for rational material engineering for a uniform memristor cell and its array application.

In this work, we systematically engineered the porosity and pore size of the nanoporous Ta_2O_{5-x} material and demonstrated a tunable switchable rectifier that is embedded with a suitable nonlinear switching feature. The material platform developed by the structural engineering exhibits an enhanced essential switching performance with low power consumption and acceptable device uniformity without significantly sacrificing the other inherent merits of NP Ta_2O_{5-x}, such as its high nonlinearity, stable pulse operation, and effective ON−OFF ratio. Specifically, we fabricated a crossbar NP Ta_2O_{5-x} memristor array by using a simple and cost-efficient process without high-temperature processing and additional integrated selectors and demonstrated the effective suppression of crosstalk between the cells.

■ RESULTS AND DISCUSSION

We fabricated NP Ta_2O_{5-x} memristor devices with different pore sizes and porosities that were engineered and designed by an electrochemical anodizing process. Figure 1a,b shows a schematic diagram of the NP Ta_2O_{5-x} memristor device with multilayer graphene (MLG, ∼10 layers) and the top-view and cross-sectional scanning electron microscopy (SEM) images of the device. To fabricate the device, Ta (200 nm)/Pt (30 nm) layers were deposited on a SiO_2/Si substrate by sputtering after the substrate was rinsed with acetone, isopropyl alcohol, and deionized water for 5 min. These metal layers were utilized as an anodizing metal (Ta) and a bottom electrode (Pt) for the memristor junction. During anodization at room temperature in a designed galvanic cell using a solution of sulfuric acid (95−98%, Sigma-Aldrich), 0.2 vol % HF (49%, Fisher Scientific), and 3 vol % H_2O, the upper Ta metal section was simultaneously oxidized and etched, which resulted in the formation of Ta_2O_{5-x} and a randomly networked three-dimensional NP structure, as shown in Figure 1b.

To engineer the porous structure of Ta_2O_{5-x}, we applied different dc voltages (40 and 50 V) for specific durations (from 5 to 30 s) in the galvanic cell. The change in the porosity and pore size depended on the applied dc voltage and the anodization time as a result of the variation in the degree of etching and oxidation of the targeted metal materials.[15,17−19] As shown in Figure 1c,d, the size and homogeneity of the pores mainly depended on the applied dc voltage, whereas the porosity was influenced by both the applied dc voltage and the anodization time.[17−20] For example, relatively small pores were observed at 40 V compared to those at 50 V for the same anodization time, which resulted in smaller porosity and little variation in their sizes (Figure S1). The porosity was estimated by the area ratio of the pores (the black areas) to the Ta_2O_{5-x} region (the white areas) on the basis of the converted high-contrast images obtained from each SEM image (the bottom images of Figure 1c). As seen in Figure 1d, the average porosity at 50 V increased and could eventually converge to a value of ∼25% as the anodization time increased, which indicates that the anodization time contributed to both the growth of the Ta_2O_{5-x} region and the formation of the pores (Figure S2).[20] These two effects that determine the porosity are inversely correlated and hence they could cause the porosity to approach a specific value. After the formation of pores in Ta_2O_{5-x}, the CVD-grown MLG film (∼10 layers) was transferred to the top of the device, and it could effectively prevent the formation of an electrical short circuit through the NP structure by the metal electrode deposited on top.[15,21] Note that the MLG film can simply act as an electrode because of the relatively high

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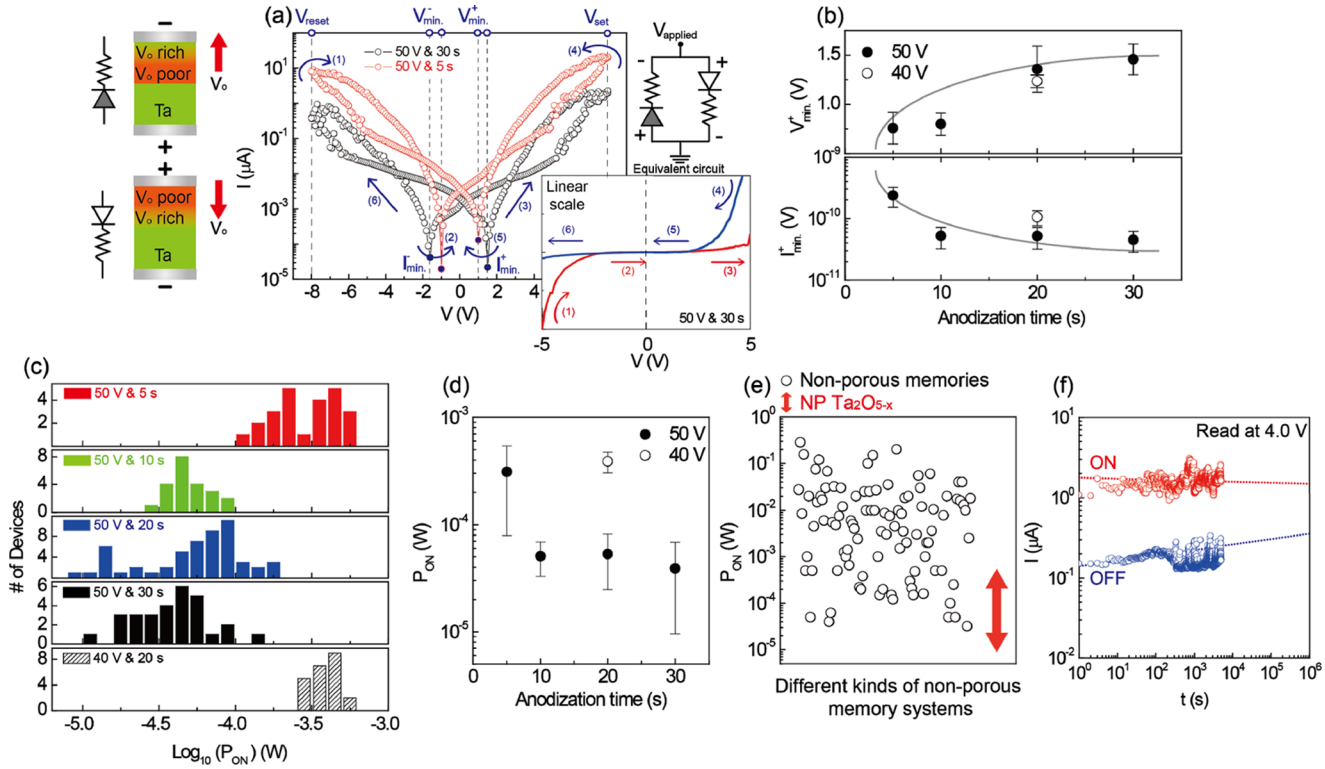

Figure 2. (a) Switching $I-V$ curves of the NP Ta_2O_{5-x} memristors fabricated at 50 V using different anodization times (5 and 30 s). The inset in the bottom right shows switchable rectifier behavior in the applied voltage range, $V \leq |5|$ V, with the equivalent electric circuit on the top right. The left schematics show the change in the $V_o^{\cdot}$ distribution of the junction structure when a positive or negative voltage is applied at the top Pt metal electrode, which results in the change of the rectifying direction due to $V_o^{\cdot}$ exchange at both interfaces. (b) V^+_{min} and I^+_{min} values. (c) Statistical histograms and the distribution of $\log_{10}(P_{ON})$, and (d) P_{ON} for different NP Ta_2O_{5-x} memristor devices fabricated under different anodization conditions. (e) P_{ON} comparison between our NP Ta_2O_{5-x} memristor (red arrow) and other nonporous memory devices (black circles). (f) Retention test of the selected Ta_2O_{5-x} memristor fabricated at 50 V for 20 s under the anodization conditions. Note that the read voltage is 4.0 V.

conductance of MLG and the negligible contact resistance of MLG/metal.[22] Then, the device was dried on a hot plate at 50 °C for 1−2 h to minimize water molecules on the internal and external oxide layers. The patterned Pt metal was sputtered on the MLG film using a shadow mask and used as a top electrode; the exposed MLG region was then eliminated by an oxygen plasma process.

Figure 2a shows the representative switching current−voltage ($I-V$) characteristics for the NP Ta_2O_{5-x} memristors fabricated at 50 V using different anodization times (5 and 30 s). They both showed switchable diode behaviors with their minimum current (I^+_{min} and I^-_{min}) values at specific positive and negative voltages (V^+_{min} and V^-_{min}), not at a zero voltage. When the voltage was sequentially swept, the corresponding current followed the sequence traces from (1) → (2) → (3) → (4) → (5) → (6) and exhibited apparent bipolar switching with set and reset voltages, as shown in Figure 2a. The observed switching behavior includes a change in the rectifying direction, which is controlled by altering the polarity and direction of the voltage sweeps; nonlinear switching dynamics are therefore observed (right bottom inset of Figure 2a).

From the depth-profiling X-ray photoelectron spectroscopy analysis, we previously confirmed the gradual reduction of the Ta_2O_{5-x} oxidation state due to different degrees of oxidation depending on the depth, which results in an oxygen vacancy ($V_o^{\cdot}$) gradient in Ta_2O_{5-x}.[15] Therefore, a gradient distribution of $V_o^{\cdot}$ already exists in the as-fabricated device; hence, asymmetric contacts such as ohmic-like (Ta_2O_{5-x}/Ta, x = ∼5) and Schottky-like contacts (MLG/Ta_2O_{5-x}, x = ∼0) are initially established at both interfaces. Similarly, for the general switching feature for a valence change memory cell that is driven mainly by the $V_o^{\cdot}$ mediator under the applied electric field,[2,4,7] the switchable diode phenomenon of NP Ta_2O_{5-x} could be attributed to the contact transition (from Schottky- to ohmic-like contacts and vice versa) at the interfaces that originates from $V_o^{\cdot}$ exchange from one interface to the opposite interface; this corresponds to the schematics on the left and the equivalent circuit on the right of Figure 2a. A similar switchable diode feature by electrical control of the $V_o^{\cdot}$ concentration at the interface between Pt and TiO_x has been investigated previously.[23] This result could also be considered to originate from the resultant variation in the Schottky barrier height by $V_o^{\cdot}$ exchange. In contrast to other switchable diode devices;[23,24] however, the abrupt decrease in the current at specific low-bias regions (the existence of I_{min}) makes the NP Ta_2O_{5-x} memristor attractive as a selector-less (or self-selecting) memory because the high resistance at V_{min} can play a pivotal role in blocking sneak current through the neighboring cells at the operating voltage schemes ($V_r/2$ or $V_r/3$ scheme).[9,14−16] This is also of considerable merit compared with previous resistive nonporous oxide-based memory devices.[2−4,6−13,25] In fact, this unique behavior can be distinguished from the general charging phenomenon often seen in the nonporous thin insulator or capacitor structures in which V_{min} values are observed mostly at zero voltage or where some are inconsistent and unsustained (Figures S3 and S4). Conversely, the NP Ta_2O_{5-x} memristor showed a marked abrupt decrease in the current (the existence of I_{min}) at a specific voltage (V_{min}) under

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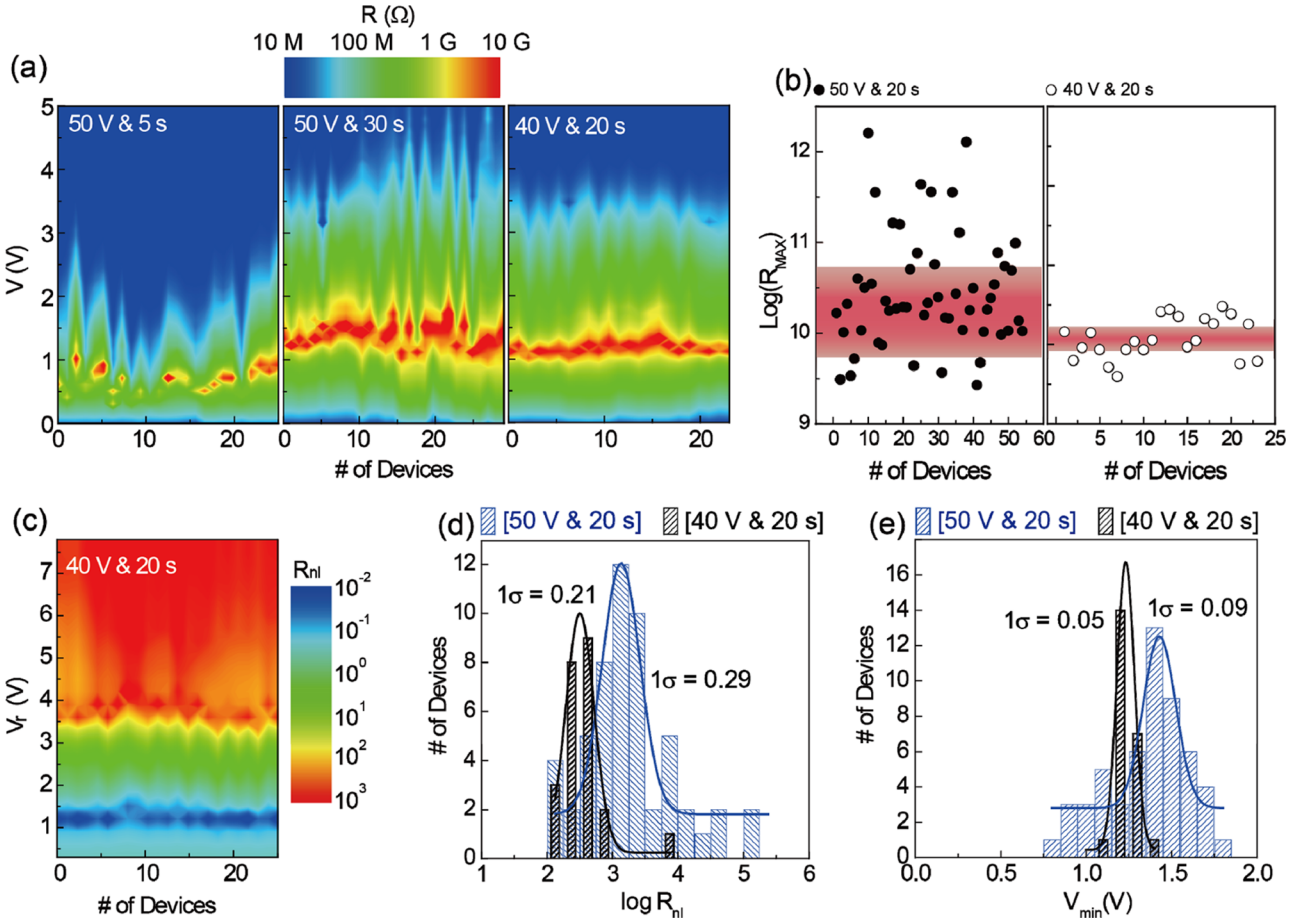

Figure 3. (a) Contour plots of the R values and their distributions for different NP Ta_2O_{5-x} memristors as functions of V and the number (#) of devices. (b) Comparison of logarithmic R_{max} values and their distribution with different anodization dc voltages (50 and 40 V) for 20 s. (c) Contour plots of the R_{nl} values for the NP Ta_2O_{5-x} memristor as functions of V_r. Comparison of statistical histograms of (d) logarithmic R_{nl} and (e) V_{min} and their standard deviations for the NP Ta_2O_{5-x} memristor with different anodization dc voltages (50 and 40 V) for 20 s.

the same measurement setup and sustained these values within a reasonable deviation during the repeated DC $I-V$ sweeps (Figure S5). We note that there are no noticeable differences in V_{min} positions even if the parasitic capacitances are changed in the different electrical measurement setups (Figures S6−S8). In addition, the main switching behavior is mostly maintained even under vacuum conditions (<10^{-3} Torr) at room temperature after vacuum annealing (∼100 °C), except for the slight shift of V_{min}, which indicates that the effect of moisture could not be a major cause of switching in the NP Ta_2O_{5-x} memristor (Figure S9).[26−28] The aforementioned experimental result was also consistent with the following two results: (i) the voltage sweep rate-independent switching curve (Figure S7) and (ii) the similar switching feature under dry air conditions (Figure S10). Note that the moisture that was absorbed in the device nanomaterials causes the voltage sweep rate-dependent hysteresis curves because of the capacitive gating effect caused by water dipoles.[29−31]

Presumably, the presence of I_{min} indicates that the partially trapped negatively charged oxygen ions in the pore or the trapped electrons in the defective oxide layer and the oxide layer with higher $V_o^{\cdot}$ concentration[32−35] can be driven by the voltage sweep to produce an internal electric field that can offset the applied external electric field; this results in the minimum conductance observed at a specific voltage. Note that the positively charged $V_o^{\cdot}$ in Ta_2O_{5-x} can effectively move along the defects and dislocations in the structure due to the high electric field gradient.[15,36,37] Therefore, the physical dimensions of the pore structure and the initial formation of a $V_o^{\cdot}$ gradient can enable the engineering of devices with both switching and rectifying functionalities because the degree of charge trapping could be mainly influenced by the different internal pore sizes, the porosity, and the magnitude of applied voltages.

Interestingly, the overall switching currents decreased and V_{min} increased when the anodization time was increased (Figure 2a,b). These phenomena could be explained by the following behavior. The anodization time determined the degree of oxidation of the Ta metal, which resulted in the increase in the Ta_2O_{5-x} region in the junction structure; hence, the overall switching currents decreased (Figures 2b and S2). In addition, by increasing the dc voltage, the larger pore size obtained could also cause further reduction in I_{min} because the pores could serve as insulating/trap barriers wherein charge transfer through the switching medium was suppressed (Figure 2b). Therefore, the increased amount of trapped charges extracted from pores with larger sizes can drive higher internal electric fields during programming, so that a higher external voltage (the increase in V_{min}) is required to suppress the charge transfer and neutralize it through the NP Ta_2O_{5-x} layer (Figure 2b). A direct relationship between the V_{min} and the applied V was observed, which can support the suggested trap-assisted switching mechanism (Figure S11). This implies that I_{min} and

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V_{min} can be predictably controlled by engineering the pores of the Ta_2O_{5-x} layer and the programming scheme, allowing for a wider operating voltage range and a controllable sneak current that determine the availability and applicability of crossbar array architectures.[6−9,11−13]

The design and fabrication of electronic memory devices for ultralow power consumption have become a key issue in modern electronic device applications because of the enormous demand for big data storage, Internet of Things applications, and the perpetual power-consuming nature of organized information in communication networks.[2,6,38−42] Figure 2c,d shows the statistical analysis of the ON power (P_{ON}) with a logarithmic scale for the NP Ta_2O_{5-x} memristor devices fabricated under different anodization conditions (∼25 individual devices for each condition). When the anodization time and the applied dc voltage were increased, the P_{ON} ($V_{set} \times I$) changed from $\sim 5.43 \times 10^{-4}$ to $\sim 0.96 \times 10^{-5}$ W due to the porosity dependence of the switching current; this change is much lower than that of other nonporous metal-oxide memories by a factor of up to $\sim 10^4$, which indicates its potential use in ultralow power memory applications (Figure 2e, Tables S1 and S2, Supporting information).[25] The porous structure in the NP Ta_2O_{5-x} device contributes to both a reduction in the overall switching conductance and an enhancement in the trapping ability, so that relatively lower P_{ON} and I_{min} (defined as the sneak current in the selector-less array scheme) values can be achieved. Notably, the standard deviation (defined as σ) of P_{ON} decreased from 0.119 to 0.07 for the normal distribution when the applied dc voltage decreased from 50 to 40 V, which indicates that a smaller and more uniform pore size results in less fluctuation of P_{ON} (Figures 2d and S12). Figure 2f shows the retention result for a selected NP Ta_2O_{5-x} memristor fabricated at 50 V for 20 s under anodization conditions. The resistances in the ON and OFF states for the NP Ta_2O_{5-x} memristors were individually measured at 4.0 V over 5×10^3 s after initially setting them at 8 V and resetting them at −8 V. Although both switching states fluctuated slightly, their ON−OFF ratios were maintained. This fluctuation might be attributed to the additional unwanted charge trapped in the pore structures during the repeated reading process. Sustaining the ON−OFF ratio during the retention test suggests that the additional charging effect induced by the repeated reading process did not significantly change the switching states, which indicates the potential applicability of the memristors for nonvolatile memory even though they should be further developed and optimized. However, the increased unwanted trapped charge and the $V_o^{\cdot}$ movement induced by the repeated high read voltage might change their original switching states, acting as destructive readout memory (Figure S13). Given all these facts, selecting the proper range of read voltages is crucial for maintaining nonvolatile switching properties of NP Ta_2O_{5-x} memory.

We note here that compared with filament-dominant switching, the interface-dominant switching transport results in the relatively low ON−OFF ratio and the reduced retention properties that are observed in the NP Ta_2O_{5-x} memristor, which have been recognized as weaknesses of interface-switching mechanisms.[2,37,43,44] In addition, the required high programming voltages and low switching speeds are the major drawbacks of our currently designed NP Ta_2O_{5-x} memristor and should be resolved to compete with state-of-the-art memristors. In contrast, the low switching currents, the good power efficiency, and the switching stability that are often observed in interface switching could be competitive strengths in low-power and robust electronic memory applications.

To evaluate the switching performance and the device-to-device uniformity for the different NP Ta_2O_{5-x} memristors, we statistically investigated the resistances and the nonlinearity of at least 25 individual devices for each anodization condition. Because of the stochastic nature of resistive switching in metal-oxide memories, the statistical approach is required to more accurately and meaningfully evaluate characteristics in oxide-based memory systems. Figure 3a shows the contour plots of the resistances for the NP Ta_2O_{5-x} memristor; the plots were obtained from linear fitting of the $I-V$ curves after applying a V_{set} = 8 V and subsequently sweeping from 8 to 0 V (the (4) direction in Figure 2a). In Figure 3a, the maximum resistances (R_{max}) are clearly located at specific positive bias regions (red in Figure 3a), and their distributions differ according to the anodization conditions. The R_{max} increased by a factor of 10 from $3.36 \pm 2.39 \times 10^9$ to $3.37 \pm 2.49 \times 10^{10}$ Ω when the anodization time increased from 5 to 30 s and slightly increased from $1.18 \pm 0.52 \times 10^{10}$ to $2.80 \pm 2.14 \times 10^{10}$ Ω when the dc voltage increased from 40 to 50 V (Figure S14). Similar to P_{ON}, the NP Ta_2O_{5-x} memristor with smaller and more uniform pores exhibited less deviation in its R_{max} values, which resulted in an improved device-to-device uniformity (Figure 3b).

Generally, the allowable size of a selector-less crossbar memory array is determined by the readout margin, defined as $\Delta V/V_{pu}$ (the pull-up voltage), which depends significantly on the magnitude of the nonlinearity value (R_{nl}), defined as the resistance ratio between $V_r/3$ and V_r or $V_r/2$ and V_r according to the schemes ($V_r/2$ and $V_r/3$ schemes, see Figure S15, Supporting Information).[9,14−16] A higher R_{nl} value results in an increase in the readout margin and can effectively reduce the probability of unwanted misreading of the switching state; hence, a crossbar array with a larger size can be achieved (Figure S16). Normally, a 10% readout margin is the minimum requirement to clearly distinguish the ON and the OFF switching states, providing the number of possible word/bit lines (N).[9,14−16] Figure 3c shows the contour plot of R_{nl} in the $V_r/3$ scheme for the selected NP Ta_2O_{5-x} memristors fabricated at 40 V for 20 s under anodization conditions. In this region, the average R_{nl} was found to be $\sim 6.39 \pm 3.53 \times 10^2$, which resulted in ∼31 Mbit for the maximum allowed number of crossbar arrays (Figure S17). Note that the $V_r/2$ scheme can also be used for the read process of the NP Ta_2O_{5-x} memristor with a different R_{nl} value, defined as the resistance ratio between $V_r/2$ and V_r (Figure S18). The details of the voltage schemes and the simulation results have been described in the Supporting Information.

The larger pore size obtained by increasing the dc voltage from 40 to 50 V can cause further increases in R_{nl}, which can result in increases in the maximum array size (Figure S16). At the same time, however, the distribution (1σ) of R_{nl}, obtained by using a Gaussian fitting, increases from 0.21 to 0.29, which is similar to the appearance of the distributions of R_{max} and V_{min} (Figure 3b,e). From this statistical analysis, we found that the pore size and homogeneity, which depend on the anodization conditions (or porosity), can affect the uniformity of the switching parameters (I_{min}, V_{min}, P_{ON}, R_{nl}, and R_{max}) due to the influence of the physical pore dimensions on charge transfer. We note here that a trade-off between the I_{min} or P_{ON} and the porosity was found, which could be utilized as a design rule for NP oxide-based selector-less switching devices (Figure S19).

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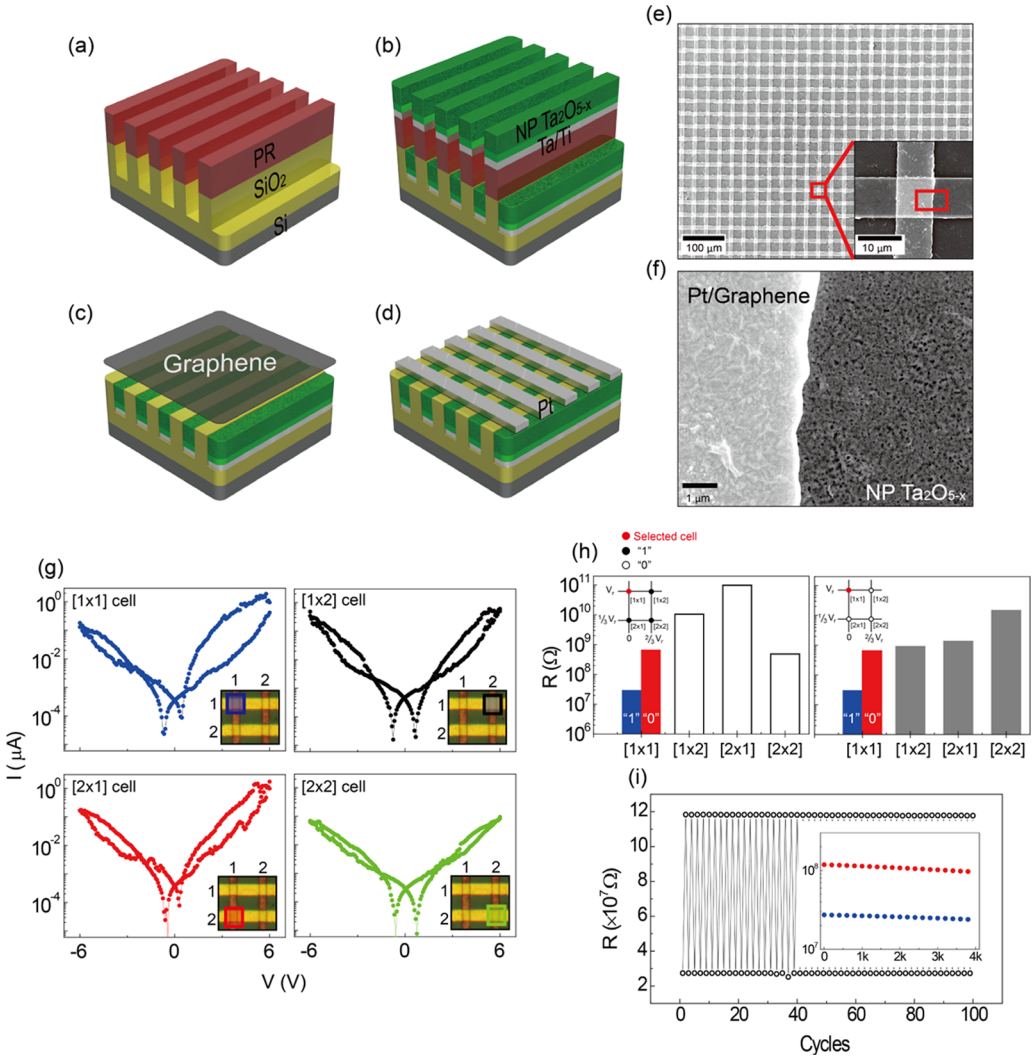

Figure 4. (a) Photolithography patterning and RIE process on the SiO_2/Si substrate. (b) Deposition of the Ta/Ti bottom electrode and anodization process of the top Ta metal on the patterned SiO_2/Si substrate. (c) Transfer of the MLG interlayer between the NP Ta_2O_{5-x} and the Pt metal for initial Schottky-like contact. (d) Deposition of the top Pt electrode on the patterned MLG/NP Ta_2O_{5-x} /Ta/Ti cell and completion of the NP Ta_2O_{5-x} selector-less crossbar device. (e) SEM and optical images of a 168 × 168 selector-less crossbar array device. (f) An enlarged SEM image of the boundary between the NP Ta_2O_{5-x} and the top Pt/MLG electrode line from a single cell of the crossbar array (marked as the red box in (e)). (g) Switching $I-V$ curves of the selected 2 × 2 selector-less crossbar array device. Average P_{on} is ~2.7 × 10^{-6} W. (h) Histograms of ON and OFF resistances of a selected cell ([1 × 1]) in the 2 × 2 selector-less crossbar array correspond to two cases in which all unselected cells ([1 × 2], [2 × 1], and [2 × 2]) are "1" or "0." V_r was set to ~2.2 V. A selected cell can be successfully switched and read as "1" for the ON state or "0" for the OFF state regardless of the states of the three unselected cells ("1" or "0"). (i) Pulse endurance tests for different cycles of a selected selector-less memory. The conduction states were programmed to be set by a writing pulse of 8 V and reset by an erasing pulse of −8 V for 500 μs, immediately followed by the reading process at 4.2 V.

As we emphasized above, the crossbar array architecture is the most desirable structure for nonvolatile two-terminal memristors because it provides the highest degree of integration for switching cells on a 2D planar substrate. We note here that the sustainability of the V_{min} and the device-to-device uniformity of our NP Ta_2O_{5-x} memristive system should be further improved for an ultrahigh-density integrated crossbar memory array. Furthermore, the controllability of pores in terms of size and uniformity should be significantly improved because it is one of most important factors in the viewpoint of rational structure design for a uniform memristor cell and its nanoscale array application. Nevertheless, this proof of concept provides an adequate means to evaluate the potential of the NP oxide-based selector-less memristor system within a reasonable crossbar density. Figure 4a−f shows the fabrication scheme, optical image, and SEM images of an NP Ta_2O_{5-x} selector-less crossbar memristor device (Figure S20). After patterning the bottom lines (~10 μm in width) using an S1813/LOR 5B bilayer photoresist stack on a SiO_2 (500 nm)/Si (750 μm) substrate (1.5 × 1.5 cm^2), a reactive ion etching (RIE) process was performed to remove the uncovered top of the SiO_2 layer (200 nm) with photoresists (Figure 4a). This process is necessary to prevent direct contact between the bottom (Ta) and top (MLG) electrode due to anisotropic etching of Ta_2O_{5-x} during the anodization etching process. Patterned Ta (200 nm)/Ti (5 nm) layers were deposited on the substrate by sputtering and then the Ta anodization process was performed at 50 V for 10 s (Figure 4b). A lift-off process was conducted using a PG remover (MICRO CHEM) to remove the residual resist. A large-scale MLG film (>1.0 × 1.0 cm^2) was transferred

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on top of the device, and then the device was dried on a hot plate at 50 °C for 1 to 2 h (Figure 4c). Top Pt (30 nm) electrodes were deposited perpendicularly at a crossing of the MLG/Ta_2O_{5-x}/Ta bottom lines, which could limit the sheet resistance of the MLG film during addressing of the memristor cell. Finally, the fabrication of the crossbar memristor device was completed by an oxygen plasma process to remove the reductant MLG region on the SiO_2/Si substrate (Figure 4d). This approach can significantly reduce the processing steps required to fabricate a crossbar array compared to those of other integrated architectures that require an additional addressing device stack such as a diode, a transistor, or a selector. Therefore, it is advantageous as a low-cost and simple approach. Furthermore, all fabrication steps were implemented at room temperature. On the basis of this method, we fabricated an NP Ta_2O_{5-x} crossbar memristor array for the proof of concept, as shown in Figure 4e,f.

To verify the exclusion of crosstalk in these structures, we first measured all the switching $I-V$ curves of 2 × 2 matrices among the NP Ta_2O_{5-x} selector-less crossbar array (Figure 4g) and designed two different reading scenarios in which all neighboring cells are ON states (denoted as "1") or OFF states ("0") (Figure 4h). By applying $V_r/3$ and $2V_r/3$ for the word and bit lines, respectively, in the 2 × 2 matrix, we found that the difference between "1" and "0" of the selected cell ([1 × 1] cell) was sufficiently distinguishable and their switching resistances (a blue box for "1" and a red box for "0" in Figure 4h) were almost independent of the switching states of neighboring cells, which indicates the effective suppression of the sneak current through unselected neighboring cells. We note here that in the $V_r/3$ scheme, the [2 × 2] cell is applied at "negative" $V_r/3$, whereas the [1 × 2] and [2 × 1] cells are both applied at "positive" $V_r/3$, as shown in the inset electric circuit in Figure 4h. In that case, the resistances of [1 × 2] and [2 × 1] are larger than those of [2 × 2] when all neighboring cells are "1" (left side of Figure 4h), whereas the resistance of [2 × 2] is larger than that of [1 × 2] and [2 × 1] when they are "0" (right-hand side of Figure 4h). Regarding the random-access operation, we used two different semiconductor parameter analyzers (B1500 and Agilent 4155C). The ON (blue histogram) and OFF (red histogram) resistances of the [1 × 1] cell were obtained from the switching $I-V$ curve measured by the B1500, whereas the word and the bit lines for the [1 × 2], [2 × 1], and [2 × 2] cells were constantly biased to $V_r/3$ and $2V_r/3$ by an Agilent 4155C after changing the states of all neighboring cells to "1" (left of Figure 4h) and "0" (right of Figure 4h), respectively. Although this measurement approach cannot entirely exclude the influence of other cells, except for selected cells in the 2 × 2 array, where the word and the bit lines are floated, the noninitialization process of the nonmeasured cells and their rectifying switching behavior can help reduce the sneak current in the array structure due to their high-resistance properties. In Figure 4i, the selected memristor cell exhibits a good pulse endurance during a few thousand cycling steps and sustains its primary switching states without a significant change in the switching resistance. The overall switching current of the crossbar array with a line width of ∼10 μm is ∼1−2 orders of magnitude lower than that of the single cell with a side length of ∼200 μm due to the interface-dominant switching mechanism. This allows it to be operated at a much lower (∼2.7 × 10^{-6} W) power than the P_{ON} range of other metal-oxide memories, as shown in Figure 2e and summarized in Tables S1 and S2.

CONCLUSIONS

In summary, we report the fabrication of a selector-less array in which the NP Ta_2O_{5-x} memristor junction is integrated at every cross-point without the need for high-temperature processing and additional selectors. Furthermore, we have demonstrated that the important switching parameters for the selector-less memory application, such as I_{min}, V_{min}, P_{ON}, R_{nl}, and R_{max}, can be modulated and further enhanced by the combination of intentional engineering of the porous structure and operational optimization, which could be applied to other NP-based memristors due to the pore-dependent switching property. The facile and low-temperature fabrication and the porous-dependent switching modulation of the NP Ta_2O_{5-x} memristor contribute to its potential for implementation in next-generation nonvolatile memory application.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b06918.

Comparison of pore size and porosity; pore and oxide region variations according to the anodization time; $I-V$ graphs; summary of ON power for nonporous oxide-based memory; statistical histograms; modeling: readout margin of the selector-less memristor crossbar array (PDF)

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Notes

The authors declare the following competing financial interest(s): J.M.T. and G.W. are co-inventors on a patent filing for Ta oxide and related memories that are selector- and diode-free. The patent rights are owned and managed by Rice University, and all potential conflicts are managed by the university's office of Sponsored Programs and Research Compliance.

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