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Three-Dimensional Networked Nanoporous Ta_2O_{5-x} Memory System for Ultrahigh Density Storage

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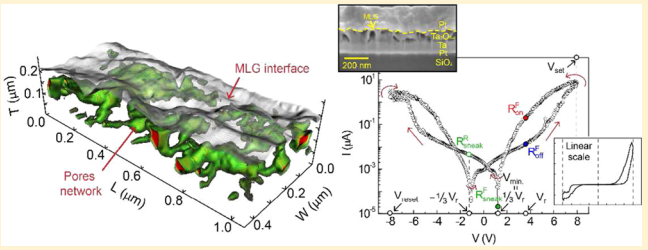
Supporting Information

ABSTRACT: Oxide-based resistive memory systems have high near-term promise for use in nonvolatile memory. Here we introduce a memory system employing a three-dimensional (3D) networked nanoporous (NP) Ta_2O_{5-x} structure and graphene for ultrahigh density storage. The devices exhibit a self-embedded highly nonlinear $I-V$ switching behavior with an extremely low leakage current (on the order of pA) and good endurance. Calculations indicated that this memory architecture could be scaled up to a ~162 Gbit crossbar array without the need for selectors or diodes normally used in crossbar arrays. In addition, we demonstrate that the voltage point for a minimum current is systematically controlled by the applied set voltage, thereby offering a broad range of switching characteristics. The potential switching mechanism is suggested based upon the transformation from Schottky to Ohmic-like contacts, and *vice versa*, depending on the movement of oxygen vacancies at the interfaces induced by the voltage polarity, and the formation of oxygen ions in the pores by the electric field.



KEYWORDS: *Nanoporous, tantalum oxide, Ta_2O_{5-x}, nonvolatile memory, resistive memory*

The interest in nonvolatile resistive oxide-based memories is grounded in the fact that such memories can offer outstanding switching performances, including faster switching speed, lower energy consumption per bit, lower manufacturing cost, and higher endurance, as well as the potential for scalability to high-density when compared to traditional Si-based memories.[1−5] By exploiting oxide-based materials, a variety of integrated architectures for a high-density array have been suggested, such as one-diode−one-resistor (1D−1R),[6−8] one-selector−one-resistor (1S−1R),[9−11] complementary resistive switch (CRS),[12−14] and three-dimensional (3D) cross-point arrays.[15] In fact, the integration of these architectures is essential for a crossbar array in order to eliminate undesirable misreading of the switching states. This occurs on the selected cell by parasitic sneak current through unselected cells, which is called crosstalk.[6−15] Many architectures show the crosstalk problems at a crossbar array over 1 Mbit in density.[6−15] For example, when the number of word/bit lines in the crossbar array is increased, the sneak current through the unselected cells and its paths are simultaneously increased, and they can then interrupt the reading process at a selected cell at a certain number of arrays.[7,9,15−17] Under these circumstances, the maximum size of the array is strictly limited. Furthermore, the fabrication of the suggested architectures often requires many prerequisite high temperature processing steps such as deposition or annealing,[6−15] which could lead to high cost and low device yields. Another important consideration is that the operating $I-V$ of the diode or selector device must be matched to the operating range of the memory device,[6−14] which can limit the number of materials available. Recently, as an effort to mitigate these issues, diverse selector-less resistive memories that show a self-embedded nonlinear $I-V$ characteristic have been suggested and investigated.[18−22] However, they still suffer from inefficient nonlinearity values that limit the maximum number of word/bit lines in the integrated array.[18−22] In addition, many of these resistive memories require multiple oxide layers. If the stoichiometry of the active materials is not tightly controlled[18−21] there could be switching nonuniformity.

In this Letter, we disclose a new design toward an ultrahigh-density nonvolatile resistive memory using a 3D networked nanoporous (NP) Ta_2O_{5-x} material that can be fabricated at room temperature. The devices show excellent selector-less memory behavior while having a much higher $I-V$ nonlinearity

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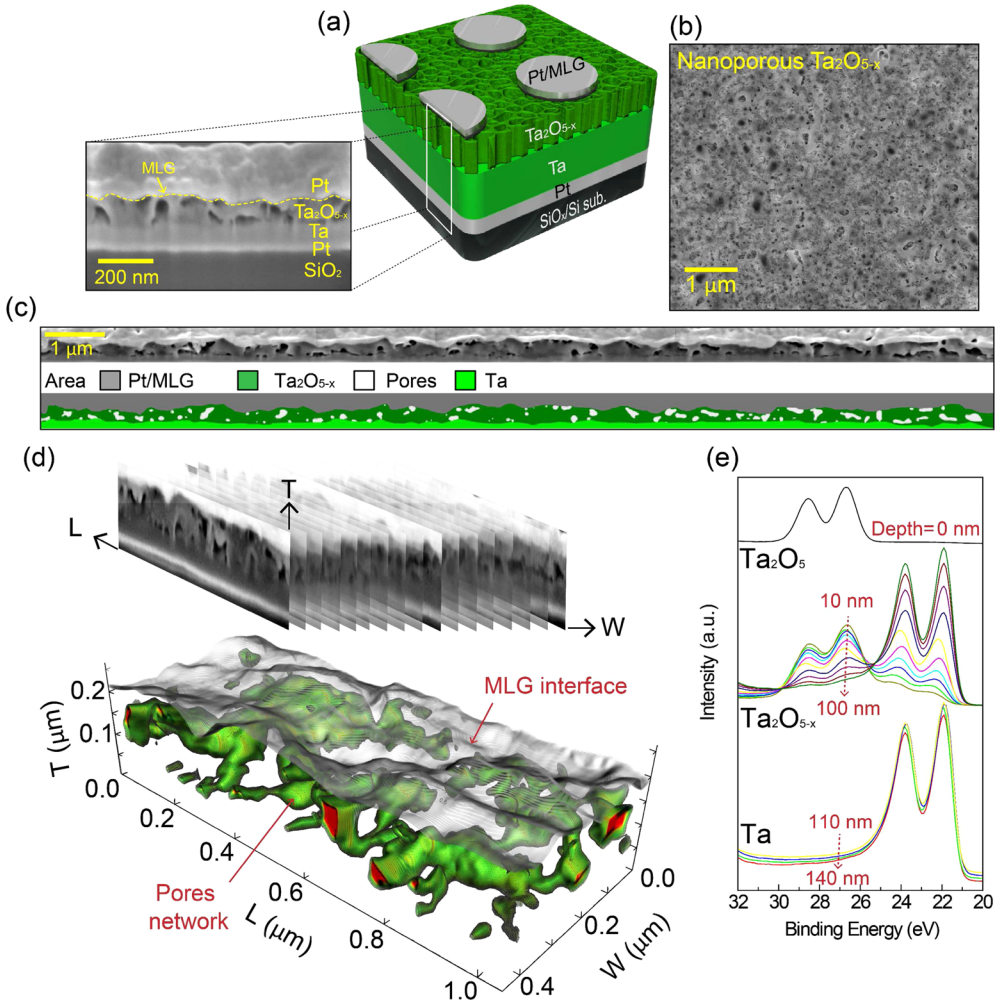

Figure 1. (a) Schematic illustration of the cells in the NP Ta_2O_{5-x} memory device with the cross-sectional SEM image at the middle of the cell. (b) Top view of SEM image of the NP Ta_2O_{5-x} film. (c) Wide-area cross-sectional image formed by joining eight high-resolution SEM images. The colored boxes in the middle of panel c correspond to the different materials detected in the SEM image for each region. (d) (top) A series of cross-sectional SEM images at intervals of 30−50 nm as functions of length (L), thickness (T), and width (W). (bottom) Three-dimensional reconstructed topology of NP Ta_2O_{5-x} junction structure, by the cross-sectional SEM images. (e) The XPS depth-profiling analysis of the Ta 4f spectra for NP Ta_2O_{5-x} film.

than present selector-less memory systems. The Ta_2O_{5-x} memory device could achieve up to a 162 Gbit crossbar array that would meet industrial requirements for highly scaled devices, which is much higher than other oxide-based memory systems currently suggested in the literature. Using this 3D networked NP Ta_2O_{5-x}, the nonlinearity value can be dramatically increased. A facile method to fabricate the resistive memory is shown without the necessity for integrating additional selectors.

Figure 1a is a schematic diagram of a 3D networked NP Ta_2O_{5-x} memory cell with multilayer graphene (MLG) and a cross-sectional scanning electron microscope (SEM) image at the middle of the cell. After the deposition of Ta (200 nm)/Pt (30 nm) on a SiO_2/Si wafer by sputtering, the NP Ta_2O_{5-x} (100 nm thick) was formed by anodization in a solution of sulfuric acid (95 to 98%, Sigma-Aldrich) with 0.2 vol % HF (49%, Fisher Scientific) and 3 vol % H_2O at 50 V for 20 s in a two electrode setup with platinum gauze as a counter electrode. The SEM image shows that the Ta_2O_{5-x} nanopores have a pore radius size distribution from 10 to 100 nm (Figure 1b). After anodization, the MLG (~10 layers grown on Cu) was transferred atop the device substrate for two reasons: first, it forms a Schottky-like barrier with the Ta_2O_{5-x} due to the band alignment.[23] Second, it effectively eliminates the formation of metal filaments through the NP layer (Figure 1a,c).[24] The average porosity value in the NP layer was ~19%, estimated by the area ratio of the pore (white color) to the Ta_2O_{5-x} region (dark green color) within a sufficiently wide cross-sectional area of the cell compared to the scale of pores (Figure 1c). The Pt metal (50 nm) was deposited atop the MLG/NP Ta_2O_{5-x} layer through a 100 μm radius shadow mask. These top and bottom Pt metals of a memory cell probably do not affect the charge transfer through the junction because the band alignment of the top or bottom contact in the junction structure is mainly determined by the location of the workfunction of MLG (Ta) and the band gap of Ta_2O_{5-x}, not by the top or bottom Pt contact. An oxygen plasma process was subsequently performed to remove the exposed MLG region. All fabrication processes were carried out at room temperature (300 K). In order to elucidate the junction topology, focused ion beam (FIB) tomography was performed by milling out the junction with slice thicknesses of 30 to 50 nm and taking cross-sectional SEM

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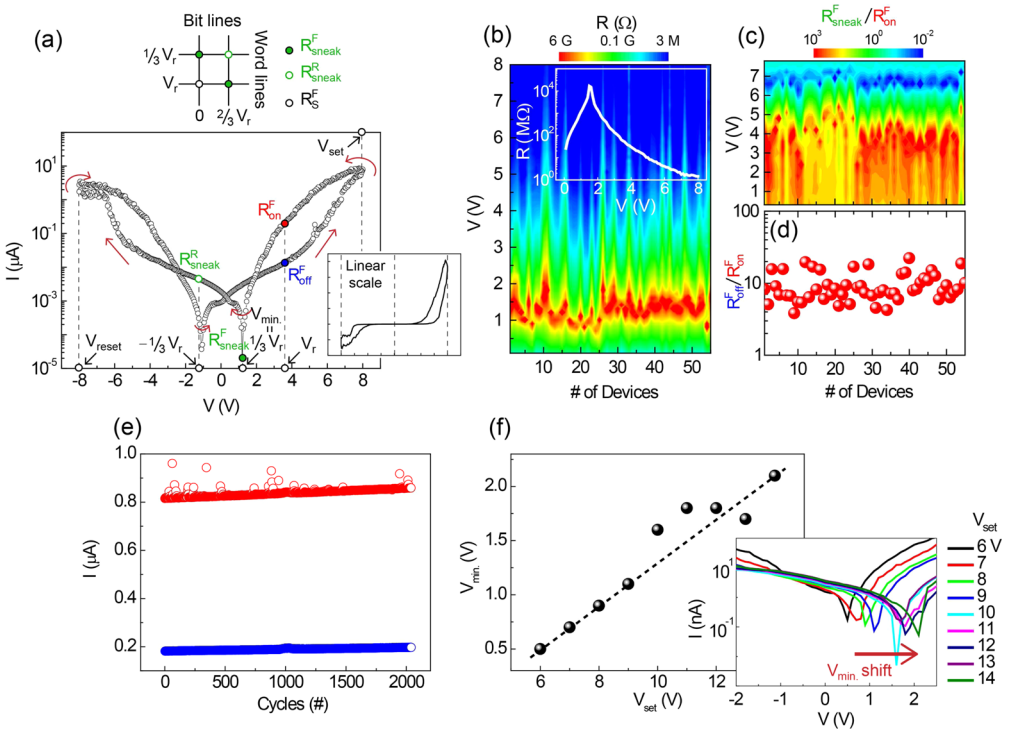

Figure 2. (a) Representative $I-V$ characteristics of the NP Ta_2O_{5-x} device with the electric circuit array for $V_r/3$ scheme (top view). (b) The contour plot of the calculated resistance R as functions of the applied voltage and the number of devices. Inset shows the representative $R-V$ curve. (c) The contour plot of the calculated nonlinearity value (R^F_{sneak}/R^F_{on}) as functions of the applied voltage and the number of devices. (d) The ON–OFF ratio (R^F_{off}/R^F_{on}) as a function of the number of devices. (e) Endurance cycling test of the selected NP Ta_2O_{5-x} device for 2×10^3 cycles. (f) The linear relationship of $V_{min}-V_{set}$ curve. Inset shows V_{min} shifts when the applied voltage is increased.

images at every milling step (Figure 1d). Based on the contrast among pores for Pt/MLG and Ta_2O_{5-x} in these SEM images (top of Figure 1d), the 3D junction structure was reconstructed. The internal pores were partially interconnected and randomly distributed (Figure 1d and Supporting Movies M1 and M2). Another interesting aspect is that the oxygen percentage of Ta_2O_{5-x} varied according to its depth, confirmed by the depth-profiling X-ray photoelectron spectroscopy (XPS) analysis with timed Ar^+ bombardment and through the Ta 4f spectra (Figure 1e). Due to the oxidation during the anodizing process, the oxygen ratio in Ta_2O_{5-x} continually decreased as the depth was increased, and it approached that of pure Ta metal at a depth of ~110 nm (Figure 1e and Figure S1 in the Supporting Information). The change of the percentages of the oxide species in Ta_2O_{5-x} leads to a distribution of TaO, TaO_2, and Ta_2O_5 species in the material.[25] Therefore, the Ta_2O_{5-x} layer forms a relative oxygen vacancy (V_o) poor/V_o rich structure depending on its depth, so that the switching could be achieved through the V_o movement between two component layers by the applied voltage polarities.[12,26,27]

Figure 2 describes the switching characteristics for the two-terminal NP Ta_2O_{5-x} memory. No electrical shorts were found in any of the devices, which implies there is no direct contact between MLG and Ta metal. In Figure 2a, a switching diode $I-V$ behavior is observed with the ON ($R^F_S = R^F_{on}$) and the OFF resistance ($R^F_S = R^F_{off}$) at a forward read voltage (V_r) controlled by different bias polarities of set voltage (V_{set}) and reset voltage (V_{reset}). The "S" and "F" of R^F_S mean the "selected" and "forward direction of voltage", respectively. Interestingly, the minimum currents of the switching $I-V$ plot exist at a certain positive and negative voltage, not at the zero voltage. This indicates that the electric field through the NP Ta_2O_{5-x} layer becomes a minimum value when a certain voltage is applied, hence the charge transfer could be mostly suppressed (*vide infra*).

In order to read out the exact data in the crossbar array, various voltage schemes for the readout process can be chosen according to the memory integration types.[9,16,17] For example, the 1D–1R array only operates in the V_r scheme, where the word and bit lines for a selected cell are biased to V_r and 0 V, respectively, while all the unselected lines are floated. In the case of 1S–1R, CRS, and the selector-less resistive memory, they can be operated in either the $V_r/2$ scheme or the $V_r/3$ scheme. The common point for these integration types is that they exhibit a lowered current at $V_r/2$ or $V_r/3$ due to their nonlinear $I-V$ behavior (inset of Figure 2a). The nonlinearity is defined as the current (or resistance) ratio between V_r and $V_r/2$ (or $V_r/3$) when the cell is in the ON-state. When the nonlinearity become very large, it can reduce the uncertainty of the unwanted misreading of the switching state in the crossbar array to an extremely low value.[9,16,17] In the $V_r/2$ scheme, $V_r/2$ is applied to all the unselected word/bit lines, while the $V_r/3$ scheme requires a relatively complicated circuitry[17] where the unselected lines were biased to $V_r/3$ for word and to $2V_r/3$ for bit lines. For a selected cell for both schemes, the selected lines were biased to V_r and 0 V (ground). Depending on the voltage schemes, the unselected cells experience only a maximum of $V_r/2$ in $V_r/2$ scheme or $V_r/3$ in $V_r/3$ scheme;[17] hence, the reading disturbance by sneak current through the $V_r/3$ scheme is less severe.

Under the $V_r/3$ scheme (top of Figure 2a), the total resistance for the sneak current in the NP Ta_2O_{5-x} memory can be determined by the sum of resistances at unselected cells that are defined as $2R^F_{sneak} + R^R_{sneak}$ in 2×2 array. When we defined

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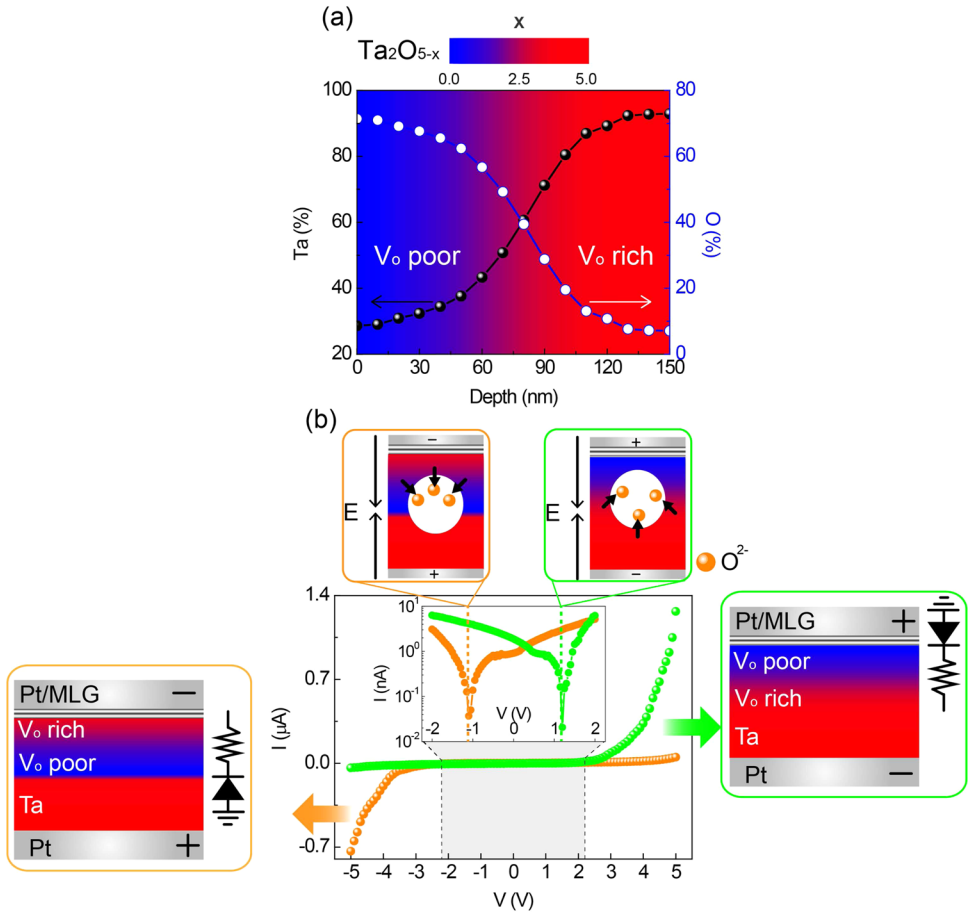

Figure 3. (a) Plots of the Ta (left) and O (right) atomic concentrations as a function of the depth of the Ta_2O_{5-x} film. Inset shows the contour plot of the calculated oxygen ratio as a function of its depth, which can form a relative V_o poor/V_o rich structure. (b) The switching diode behavior when the applied voltage is changed from 5 V to −5 V or from −5 to 5 V with the equivalent circuits of Pt/MLG/NP Ta_2O_{5-x}/Ta junction structures. The left and right schematics indicate the junction structures with the different distribution of V_o when a positive or negative voltage at the interface of the Pt/MLG/NP Ta_2O_{5-x} is initially applied, respectively. The inset in the central figure shows the enlarged semilog plot of $I-V$ at the low bias regime under different voltage polarities. The top schematics indicate the junction structure with the negative oxygen ions in the pores driven by the electric field. The negative oxygen ions can be driven until the electric field across the junction is offset.

the voltage position for maximum resistance as $V_r/3$ (1.2 V), the ON−OFF ratio at V_r (3.6 V) is slightly higher than 10 (Figure 2a). The nonlinearity value in Figure 2a (R^R_{sneak}/R^F_{on}) is found to be more than 10^4, which allows them to extend to >7 Gbit crossbar array (see Figure S2, Supporting Information).

In order to evaluate the uniformity of switching in the NP Ta_2O_{5-x} memory, we statistically investigated the resistances, the nonlinearity, and the ON−OFF ratios of ∼55 devices (Figure 2b−d). After applying the V_{set} = 8 V and sweeping from 8 to 0 V, the resistances were calculated from the linear fit of $I-V$ data for each device, as shown in the contour plot in Figure 2b. We found that the maximum resistances (∼10 GΩ) in forward bias appear in the voltage range from 1.2 to 1.7 V (red region in Figure 2b) defining R^F_{sneak} at $V_r/3$ scheme, a representation of which is shown as the inset of Figure 2b. The average V_r for maximum nonlinearity is ∼4.25 ± 0.30 V, and the average nonlinearity is ∼1.8 × 10^3 (Figure 2c). The ON−OFF ratio at this V_r was found to be ∼9.53 ± 4.37, which is similar to that of other Ta_2O_5 memories (Figure 2d).[12,20,26] This means that the NP Ta_2O_{5-x} memory can switch without significant loss of its ON−OFF ratio. However, the set/reset currents at the operation voltages are much lower than that of other Ta_2O_5 memories by a factor of up to 10^2, suggesting its promising potential for an ultralow power memory.[12,20,26] We suspect that the variation of the pore structure, depending on the porosity and pore size, is one cause of the fluctuations in the switching parameters. In Figure 2e, structures show good endurance during 2000 cycles without any significant fluctuation of the states. The conduction states were programmed to be set by a writing pulse of 8 V and reset by an erasing pulse of −8 V during 500 μs, immediately followed by the reading process at 4.2 V.

Figure 2f shows the voltage position (V_{min}) for a minimum current (or maximum resistance) of a NP Ta_2O_{5-x} memory as a function of the applied V_{set}. An apparent linear relationship between V_{min} and V_{set} was observed, which means it can be switched using different operating voltage regimes and give a wider range of switching characteristics in power consumption and ON−OFF ratios (see Figure S3, Supporting Information). When the V_{set} was increased, the V_{min} increased while the minimum current remained mostly unaffected (inset of Figure 2f). This linear relationship supports the idea that the switching mechanism is related to the presence of oxygen ions in the pores, depending on the external electric field. Higher V_{set} could drive more oxygen ions to the relatively V_o poor part of the pores. The negatively charged oxygen ions could produce an internal electric field that could balance with the external electric field at a certain voltage point. This indicates that the

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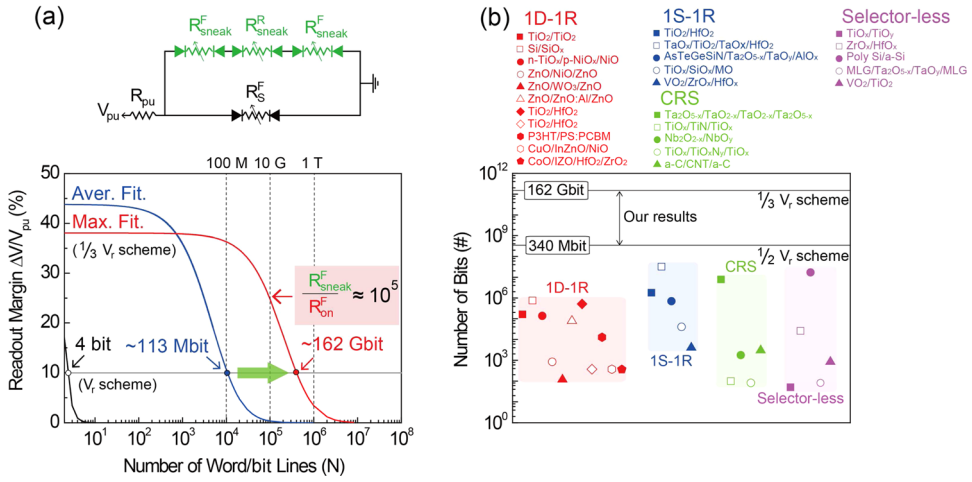

Figure 4. (a) Calculated readout margin $\Delta V_{out}/V_{pu}$ as a function of the number of word/bit lines for NP Ta_2O_{5-x} memory system under V_r scheme and $V_r/3$ scheme. The blue or red line indicates the result of the readout margins that are calculated based on the average (blue) or maximum (red) nonlinearity value of the NP Ta_2O_{5-x} memory system. (b) The maximum size of bits for the NP Ta_2O_{5-x} memory system under $V_r/2$ scheme and $V_r/3$ scheme and for other integrated architectures such as 1D−1R, 1S−1R, CRS, and selector-less memory systems under V_r scheme or $V_r/2$ scheme.

minimum currents through the NP Ta_2O_{5-x} memory may exist at a certain voltage point, not at zero voltage.

To better understand the switching mechanism behind the switching diode behavior and the presence of minimum current at a certain voltage, we constructed a contour plot of the estimated oxygen ratio for Ta_2O_{5-x} as a function of its depth based on measured Ta and O atomic concentrations by XPS profiling analysis (Figure 3a). Since the oxygen ratio is inversely proportional to the V_o, the V_o was gradually increased when the NP Ta_2O_{5-x} was deeper, thereby separating the V_o poor and V_o rich areas in the film (Figure 3a). In the bias regime from −5 to 5 V, contour plots clearly exhibited the change of rectifying direction according to the sweep direction of applied voltage (Figure 3b), which indicates the polarity switch of the Schottky diode. This switchable diode behavior can be understood by the Schottky-like barrier modulation induced by the V_o exchange from one interface to the opposite interface and *vice versa*, depending on the bias polarity and its magnitude. When V_o is concentrated at one end of the NP Ta_2O_{5-x}, an Ohmic-like contact can be formed due to the relatively low contact barrier, and then they established asymmetric contacts with a Schottky-like contact at another interface. In a low bias regime (V < |2| V), the current rises to a minimum value at certain voltages. We speculate that the negatively charged oxygen ions could be pulled from the surface of the pores and confined to pores when the voltage is applied, which affects the strength of electric field across the NP Ta_2O_{5-x}. When the electric field induced by oxygen ions matches the external electric field, the transport charges are difficult to move, causing a minimum current at certain voltages, as shown in the top schematics of Figure 3b. Therefore, higher set voltages V_{set} are the cause of an increase in V_{min}, which explains the linear relationship of the $V_{min} - V_{set}$ plot in Figure 2f.

The readout margin simulation determines the maximum size of the array.[7,9,16,17] Figure 4a shows the calculated readout margin of the NP Ta_2O_{5-x} memory with various voltage schemes using the crossbar array equivalent circuits (the top of Figure 4a). We assumed a "worst-case scenario" where all unselected cells were ON-states with negligible line resistances, incurring maximum disturbance in reading process, the so-called one bit-line pull-up (one BLPU).[9,16] Under this circumstance, the voltage drop (ΔV) difference across the pull-up resistor (R_{pu}) in the crossbar array can be used to distinguish between the ON- and OFF-states of the selected cell. Generally, $\Delta V/V_{pu}$ (pull-up voltage) = 10% has been known as a minimum criterion to differentiate their switching state,[7,9,16] which can provide the maximum number (N) of its word/bit lines using the resistor voltage divider eq 1 as follows:

$$\frac{\Delta V}{V_{pu}} = \frac{R_{pu}}{\left[R^F_{on} \left|\right| \left(\frac{2R^F_{sneak}}{(N-1)} + \frac{R^R_{sneak}}{(N-1)^2}\right)\right] + R_{pu}} - \frac{R_{pu}}{\left[R^F_{off} \left|\right| \left(\frac{2R^F_{sneak}}{(N-1)} + \frac{R^R_{sneak}}{(N-1)^2}\right)\right] + R_{pu}} \quad (1)$$

In our case, the R^F_{sneak} and R^R_{sneak} at unselected cells can determine the total resistance through sneak paths, which can be obtained from the $I-V$ curves by the linear fittings. Assume that the resistance of the R_{pu} was set to R^F_{on} at V_r (4.5 V) to achieve the maximum readout margin. Depending on the voltage schemes, the allowed maximum number of crossbar array would be significantly increased from four bit for V_r scheme and 113 Mbit for $V_r/3$ scheme on average (Figure 4a). If we choose the experimental $I-V$ data having a highest nonlinearity close to ~10^5, the NP Ta_2O_{5-x} memory can be further scaled up to a ~162 Gbit crossbar array (Figures 4a and S4). Figure 4b shows the comparison of the calculated maximum number of bits for various kinds of integrated architectures such as 1D−1R, 1S−1R, CRS, and selector-less memory based on their best $I-V$ plots, respectively (see Table S1 in the Supporting Information).[28] As shown in Figure 4b, the maximum allowed number of bits for the NP Ta_2O_{5-x} under $V_r/2$ scheme or $V_r/3$ scheme is much higher than any of these previous reported systems without a requirement of selectors and diodes, suggesting an ultrahigh density storage technology.

In summary, an oxide-based memory system using NP Ta_2O_{5-x} has an excellent self-embedded highly nonlinear $I-V$ switching behavior, which could be integrated up to ~162 Gbit,

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far beyond current architectures for two-terminal resistive memory. It can be fabricated at room temperature and consumes relatively low power when compared to other Ta_2O_{5-x} memory devices. In addition, depending on the operating voltages, the location for V_{min}, the power consumption, and the ON−OFF ratio can be changed. The switching mechanism can be explained by a transformation from Schottky- to Ohmic-like characteristics at the interfaces of MLG/NP Ta_2O_{5-x}/Ta, and *vice versa*, and the confined negatively charged oxygen ions in the pores. Our results suggest that the NP Ta_2O_{5-x} memory system could offer a new device platform for future ultrahigh density memory applications.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b02190.

Oxygen ratio, readout margin, switching properties under various set voltage, and comparison of switching parameters for other integration architectures (PDF)

Cross-sectional SEM images at every milling step (AVI)

Rotating 3D reconstructed topology of NP Ta_2O_{5-x} junction structure, by the cross-sectional SEM images (AVI)

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Author Contributions

G.W. designed and performed the experiments and wrote the manuscript. J.-H.L., Y.Y., G.R., and Y.J. assisted in measurement, device fabrication, and analysis. N.D.K. synthesized the multilayer graphene. All authors interpreted the data and wrote the manuscript. J.M.T. planned and supervised all phases of the project and corrected the manuscript.

Notes

The authors declare the following competing financial interest(s): J.M.T., G.W., and Y.Y. are co-inventors on a patent filing for Ta oxide and related memories that are selector- and diode-free. The patent rights are owned and managed by Rice University.

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(28) The switching parameters from the literature are summarized in the Supporting Information (Table S1).

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