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ARTICLE

# Conducting-Interlayer $SiO_x$ Memory Devices on Rigid and Flexible Substrates

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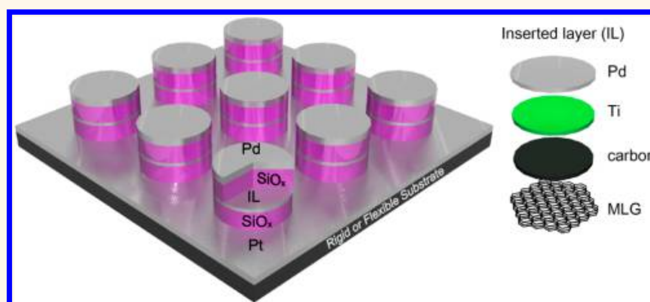
**ABSTRACT** $SiO_x$ memory devices that offer significant improvement in switching performance were fabricated at room temperature with conducting interlayers such as Pd, Ti, carbon, or multilayer graphene. In particular, the Pd-interlayer $SiO_x$ memory devices exhibited improvements in lowering the electroforming voltages and threshold voltages as the number of inserted Pd layers was increased, as compared to a pure $SiO_x$ memory structure. In addition, we demonstrated that the Pd-interlayer $SiO_x$ junction fabricated on a flexible substrate maintained low electroforming voltage and mechanically stable switching properties. From these observations, a possible switching mechanism is discussed based on the formation of individual conducting paths at the weakest edge regions of each $SiO_x$ film, where the normalized bond-breaking probability of $SiO_x$ is influenced by the voltage and the thickness of $SiO_x$. This fabrication approach offers a useful structural platform for next-generation memory applications for enhancement of the switching properties while maintaining a low-temperature fabrication method that is even amenable with flexible substrates.




**KEYWORDS:** $SiO_x$ · nonvolatile memory · RRAM · electroforming · flexible memory · conducting-interlayer $SiO_x$ memory

Two-terminal resistive random access memory (RRAM) has been highlighted for the development of next-generation nonvolatile memory because of its excellent scalability within a simple structure, high switching speed, low programming energy per bit, and high endurance.[1−5] A wide variety of materials exhibiting resistive switching behavior such as metal oxides,[6−10] silicon oxide,[11−14] amorphous Si,[15,16] organic materials,[17−19] and nanocomposites[20] have been investigated as candidates for inclusion in future memory devices. In addition, various mechanisms have been suggested to better understand the switching behaviors.[21−26] For example, in many oxide-based RRAMs, it is thought that the switching behavior is mainly attributed to the formation and rupture of nanoscale conductive filaments within the insulating oxide medium, with two representative switching modes (unipolar and bipolar), based on the applied voltage and its polarity.[22−27] The nanoscale conductive path offers the possibility of scaling the memory cell substantially beyond that attainable by scaling of traditional complementary metal oxide semiconductor (CMOS) memories.[26,27]

In order to initially activate the pristine resistive memory into the switching states, the memory cell requires high voltage stress for the formation of the localized semipermanent conducting path (or filament) at the edge (or inside) of the insulating medium, which is generally referred to as the electroforming process.[26−30] The required high voltage for the forming process, however, could cause permanent damage to the oxide-based memory material itself, which would limit the switching performance and the device yield suitable for future memory applications.[26,31,32] In addition, the electroforming process could restrict the integration potential for advanced crossbar architectures such as one diode−one resistor (1D-1R) and one selector−one resistor (1S-1R) designs because the high voltage could adversely affect the electrical properties of the oxide-based diode and the selector as well as even a Si diode.[31−34]

To reduce the electroforming voltage ($V_{forming}$) of metal oxide memory while enhancing the switching performances, various methods have been developed.[11,22,23,30,31,35,36] However, many methods commonly involve

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high-temperature processes such as deposition[22,35] or thermal annealing treatments[11,23,30,36] that are not easily applied to a stackable integration with a diode or selector on each cell.[6,34,37] High-temperature processes can degrade the electrical properties of previously deposited diode, selector, or memory layers and also result in higher fabrication cost due to the increased thermal budget.[6,34,37] Furthermore, high-temperature processes are not appropriate for memory applications on flexible substrates due to the thermal instability of those platforms.[38−40] Therefore, in order to meet these desirable requirements for future two-terminal RRAM, it is necessary to find (a) a new approach for the enhancement of the switching properties and (b) a low-temperature fabrication method that does not degrade the switching performances.

We have previously demonstrated a unipolar resistive $SiO_x$ ($1 \le x < 2$) memory device and a highly integrated crossbar structure for 1D-1R devices.[11,12,14,26] However, without high-temperature annealing treatment, every cell on the device required $V_{forming}$ to be >20 V for the initial switching activation. In this report, we demonstrate a simple approach to remedy the need for high $V_{forming}$ by fabricating $SiO_x$ memory devices using a conducting interlayer such as Pd, Ti, carbon, or multilayer graphene (MLG) inside the $SiO_x$, and the interlayer material was deposited at room temperature. The switching properties of the conducting-interlayer $SiO_x$ memory were statistically investigated and improved. Of the interlayer materials tested, the Pd-interlayer $SiO_x$ memory devices had the best performance, demonstrating improvements in $V_{forming}$, threshold voltages ($V_{th}$), and switching speed as compared to the pure $SiO_x$ memory. This was achieved without degradation of ON−OFF ratios or stability. In addition, we demonstrated that the Pd-interlayer $SiO_x$ memory can be fabricated on flexible substrates with low $V_{forming}$, and they can operate under mechanical stress with consistent switching properties. We developed a comprehensive explanation for the reduction of $V_{forming}$ with a conducting-interlayer $SiO_x$ memory system based on the normalized bond-breaking probability of $SiO_x$ according to the applied voltage and the thickness of $SiO_x$. This study will lead to further developments in the practical integration of $SiO_x$ and other oxide-based memories in terms of the enhancement of the switching performances and the low-temperature fabrication method.

## RESULTS AND DISCUSSION

Figure 1a,b is a schematic diagram of the $SiO_x$ memory cell with different conducting inserted layers (IL) such as Pd, Ti, carbon, or MLG. Similar approaches using the insertion of an oxidizable metal layer (Cu) in $ZrO_2$ resistive memories have been reported.[41,42] However, to our knowledge the use of conducting interlayers has never been demonstrated in $SiO_x$ memories. In order to fabricate the conducting-interlayer $SiO_x$ memory device, Pt metal (20 nm) was used as a bottom electrode by sputter deposition on a p-type (100) Si wafer (1.5 cm × 1.5 cm) covered with thermally grown 300-nm-thick $SiO_2$. Then, photoresist was spin-coated on the samples, and circular memory elements were patterned using typical UV-mask photolithography. The Pd-interlayer $SiO_x$ memory cell was formed from the deposition and liftoff of Pd (40 nm)/$SiO_x$ (30 nm)/Pd (5 nm)/$SiO_x$ (30 nm) on the Pt/$SiO_2$/Si substrate using e-beam evaporation. All fabrication processes were performed at room temperature (300 K). Figure 1c shows a scanning electron microscope (SEM) image of the Pd-interlayer $SiO_x$ memory with an enlarged SEM image inset. The junction radii in this study are 25 and 50 $\mu$m. We also fabricated $SiO_x$ memory with different numbers of the inserted Pd interlayers, as shown in Figure 1d. From the cross-sectional SEM image shown in Figure 1d, the Pd-interlayer $SiO_x$ memory was successfully fabricated with minimal migration of Pd metal atoms into the active $SiO_x$ memory layers. Additional details on the fabrication process for other conducting-interlayer $SiO_x$ memory devices are provided in the Supporting Information (Figures S1 and S2 and Materials and Methods section). All electrical characterizations were performed under vacuum (~$10^{-5}$ Torr) using Agilent 4155C and B1500 semiconductor parameter analyzers equipped with a pulse generator.

Typically, the electroforming process for $SiO_x$ memory can be achieved by voltage sweeps to a certain high value where the conductance suddenly increases, which is referred to as the $V_{forming}$.[11,26] The voltages for the increase in conductance and the current fluctuation gradually moved to the lower voltage region in the subsequent voltage sweeps. Finally, reproducible switching $I-V$ behaviors were revealed (Figure S3). There is no noticeable size-dependent electrical behavior due to the switching behavior being by a conducting nanofilament at a sub-5-nm scale (Figure S4).[26] It has previously been demonstrated that the electroforming process in $SiO_x$ memory involves the local enrichment of Si nanocrystals (NCs) from the $SiO_x$ matrix at the edge of the junction.[11,26] The conducting path is formed by conducting phase Si NCs, and the switching is controlled by the transition between the conducting Si NCs and an amorphous Si form, with the set and reset processes driven by an electric field and Joule heating, respectively.[26]

We fabricated and characterized a large number of Pd-interlayer $SiO_x$ memory devices (203 devices in total) to statistically analyze their electronic switching properties (Figure 2). The switching properties for other conducting (Ti, carbon, or MLG)-interlayer $SiO_x$ memories are provided in the Supporting Information (Figures S5−S7). At the outset of this study, we expected that the different work functions of the conducting-interlayers (Pd ≅ 5.22 to 5.6, C ≅ 5, MLG ≅ 4.5 to 4.8, Ti ≅ 4.33 eV) would affect the switching properties

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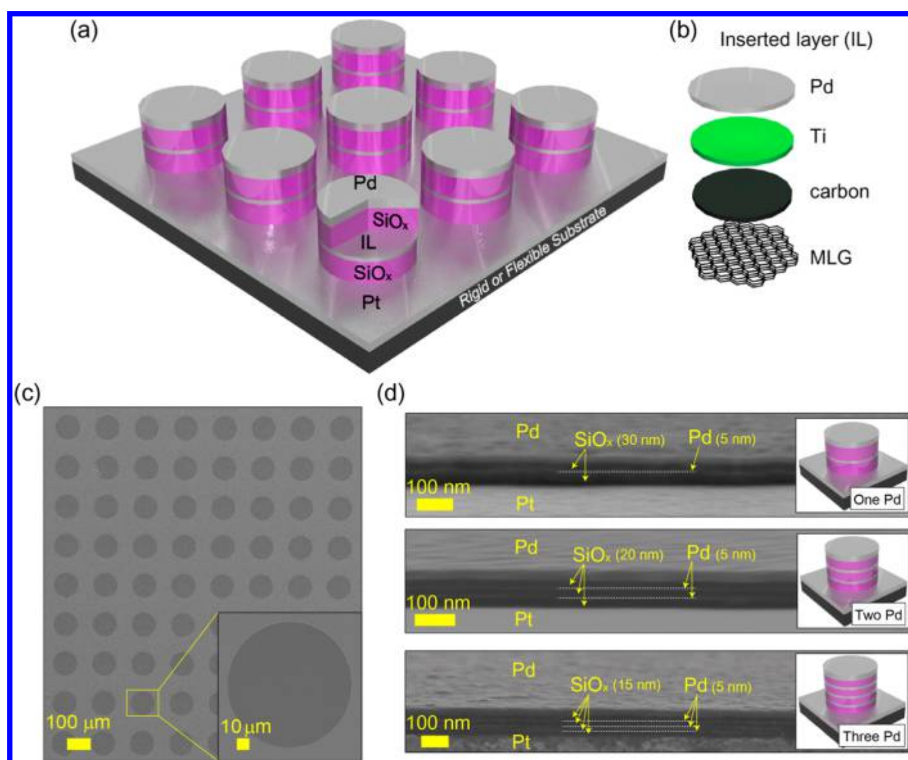


**Figure 1. (a) Schematic illustration of the cells in the conducting-interlayer $SiO_x$ memory device. (b) Four types of inserted conducting layers were used: Pd, Ti, carbon, and multilayer graphene (MLG). (c) SEM image of the Pd-interlayer $SiO_x$ memory devices. The radius of the devices is 50 $\mu$m. The inset shows a junction cell. (d) Cross-sectional SEM image of the Pd-interlayer $SiO_x$ memory devices with the schematic images for different numbers of Pd interlayers.**

of $SiO_x$ due to the different band alignment with the conducting Si-filament in the $SiO_x$ layer. However, we found that the electrical switching performance was more significantly affected by the voltage stability or the oxidation of the conducting material and by the fabrication procedure. For example, in the case of Ti-interlayer $SiO_x$ devices, most of them do not show the electroforming process even though a high voltage (∼20 V) was repeatedly applied. This might be due to the oxidation of Ti at the edge of the junction, resulting in an additional insulating barrier (Figure S5). In contrast, many MLG-interlayer $SiO_x$ devices show electrical shorts after a few voltage sweeps, a process referred to as hard breakdown, due to the prerequisite annealing process involved in its fabrication (Figures S2 and S6). In case of the carbon-interlayer $SiO_x$, it shows a large fluctuation in endurance behavior because the carbon layer could be partially decomposed during the repeated voltage stress due to the weakness of the amorphous layer (Figure S7).

Figure 2a shows the representative initial $I-V$ curves for different numbers of Pd interlayers during the electroforming process. As shown by the arrows in Figure 2a, the $V_{forming}$ is significantly decreased when the number of inserted Pd layers was increased. Figure 2b shows the statistical histogram of $V_{forming}$ for Pd-interlayer $SiO_x$ memory systems (203 different cells) with the fitting curves by Gaussian functions. The $V_{forming}$ were found to be $21.1 \pm 0.8$, $12.1 \pm 3.7$, $8.9 \pm 3.2$, and $8.3 \pm 2.3$ V for zero, one, two, and three layers of Pd inside the $SiO_x$ layer, respectively. The $V_{forming}$ and the switching currents ($I_{ON}$ and $I_{OFF}$) of one-Pd-interlayer $SiO_x$ memory are similar to the one-Pt-interlayer $SiO_x$ memory, which means Pd and Pt play a similar role as a conducting interlayer in the $SiO_x$ layers (Figure S8). We also found that the Pd-interlayer $SiO_x$ memory shows much lower $V_{forming}$ than that of the pure $SiO_x$ memories though device to device variability increased. The average $V_{forming}$ of the three-Pd-interlayer $SiO_x$ memory devices was lower by >60% as compared to the pure $SiO_x$ memory devices. This $V_{forming}$ is also the lowest value recorded for $SiO_x$ memory systems made by different fabrication methods or through treatment by thermal annealing.[11,22,35,36]

Furthermore, we observed that the electrical switching properties such as the ON−OFF current level, the threshold voltage for the set process, and the switching speed were impacted by the number of inserted Pd layers, as shown in Figures 2c,d and 3a,b, while the ON−OFF ratio (∼$10^5$) remained approximately constant, as shown in Figure 2c,d. The ON−OFF ratio is determined by the growth and shrinkage of the Si NCs in a local region (∼5 nm) in the conducting filament by response to different electrical stimuli.[26] Therefore, the ON−OFF ratio for the Pd-interlayer $SiO_x$ memory can remain almost the same regardless of the number of inserted Pd layers. Figure 2c shows the switching $I-V$ curves of the Pd-interlayer $SiO_x$ memory devices based

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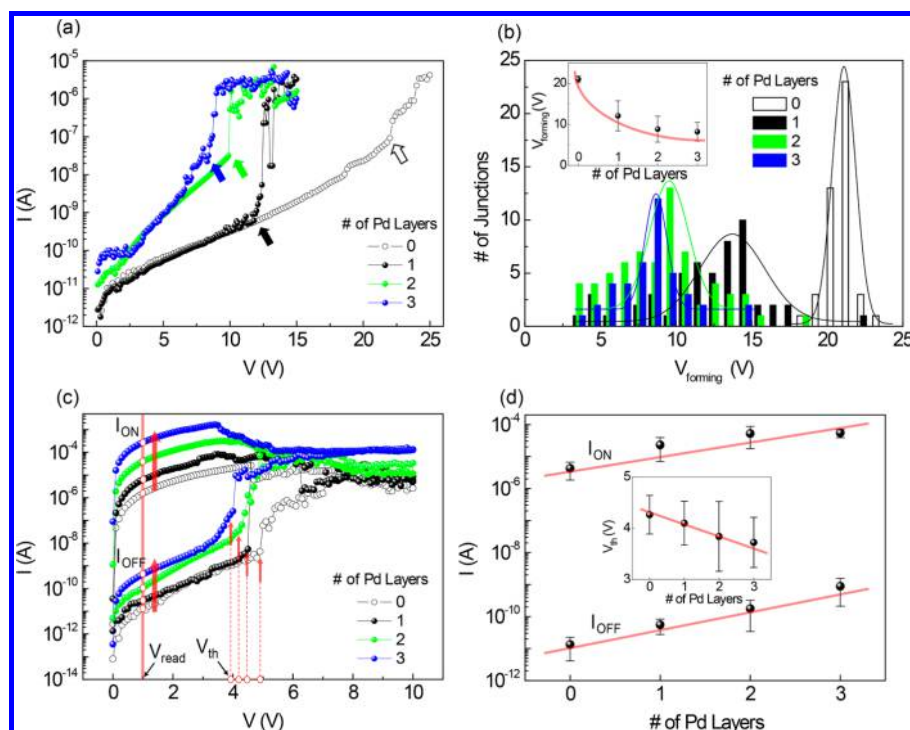


**Figure 2. (a) $I-V$ curves for different numbers of Pd-interlayer $SiO_x$ memory devices during the initial electroforming process. (b) Statistical histogram of the $V_{forming}$ for 203 different cells with different numbers of Pd-interlayers in the $SiO_x$ memory devices. The fitting curves were obtained by Gaussian functions. The inset shows the plot of $V_{forming}$ as a function of the Pd layers. The error bars in the inset represent the standard deviation across all tested device cells (more than 50 cells for each number of Pd layers). (c) Representative switching $I-V$ characteristics for different numbers of Pd interlayers in $SiO_x$ memory devices. The red arrows indicate the increase of $I_{ON}$ and $I_{OFF}$ and the decrease of $V_{th}$ when the number of inserted Pd layers was increased. (d) Semilog plots of $I_{ON}$ and $I_{OFF}$ for the Pd-interlayer $SiO_x$ memory devices *vs* the different number of Pd layers. The inset shows the $V_{th}$ according to the different number of Pd layers.**

on the different number of Pd layers after the electroforming process. They all show unipolar switching behavior, which can be programmed for the ON and OFF state by applying the same voltage polarity,[4,11] with positive operating read, set, and reset voltages. The unipolar behavior can exclude the switching mechanism by metal ionic motion in the $SiO_2$ layer.[43] In the $I-V$ curves for the pure $SiO_x$ memory, the current levels suddenly increase at ~5 V ($V_{th}$) to a low resistance state (LRS) from a high resistance state (HRS), and they then fluctuate above ~8 V. These two voltages can be defined as the set and reset voltages, respectively.[11] The red circles in Figure 2c indicate the ON currents ($I_{ON}$) and OFF currents ($I_{OFF}$) at the read voltage of 1.0 V and the $V_{th}$ for different numbers of Pd-interlayer $SiO_x$ memory systems. As shown in Figure 2c,d, the $I_{ON}$ and $I_{OFF}$ are increased and the $V_{th}$ is decreased when the number of inserted Pd layers was increased.

Interestingly, we also observed that the minimum pulse widths for the complete set processes were reduced when the number of inserted Pd layers was increased (100 ns to ≤50 ns), as shown in Figure 3a,b and Figure S9. In the pure $SiO_x$ memory device (Figure 3a), they can be set to different ON states by the different pulse widths of 50 and 100 ns at 4.5 V, while they all can be reset by a 50 ns pulse at 12 V. When the pulse width for the set process was increased from 50 ns to 100 ns, it can more completely set the device into the LRS due to the larger formation of the conducting filament.[12] We have not observed the 50 ns pulse width for the complete ON state in the pure $SiO_x$ memory devices.[12] In the three-Pd-interlayer $SiO_x$ memory device (Figure 3b), however, the minimum pulse widths for complete LRS and HRS were found to be 50 ns at 4.5 V and 50 ns at 10 V, respectively; there were no intermediate ON states. As the pulse width is shortened to tens of nanoseconds, the output signal can be distorted due to the parasitic impedance components of the measurement system (*i.e.*, contact resistance and capacitance of the device) and impedance mismatch.[43,44] Although the output pulse width could not be estimated, it was confirmed that after sub-50 ns of pulse was applied to the Pd-interlayer $SiO_x$ memory device, the states were completely changed. The pulse widths that we applied are at the resolution limit of the Agilent B1500, and there is no difference in switching speeds between the two-Pd-interlayer $SiO_x$ and the three-Pd-interlayer $SiO_x$ memory systems (Figure S9), so there is a chance that the Pd-interlayer $SiO_x$ memory may operate at even faster switching speeds. But, in order to apply and measure the more

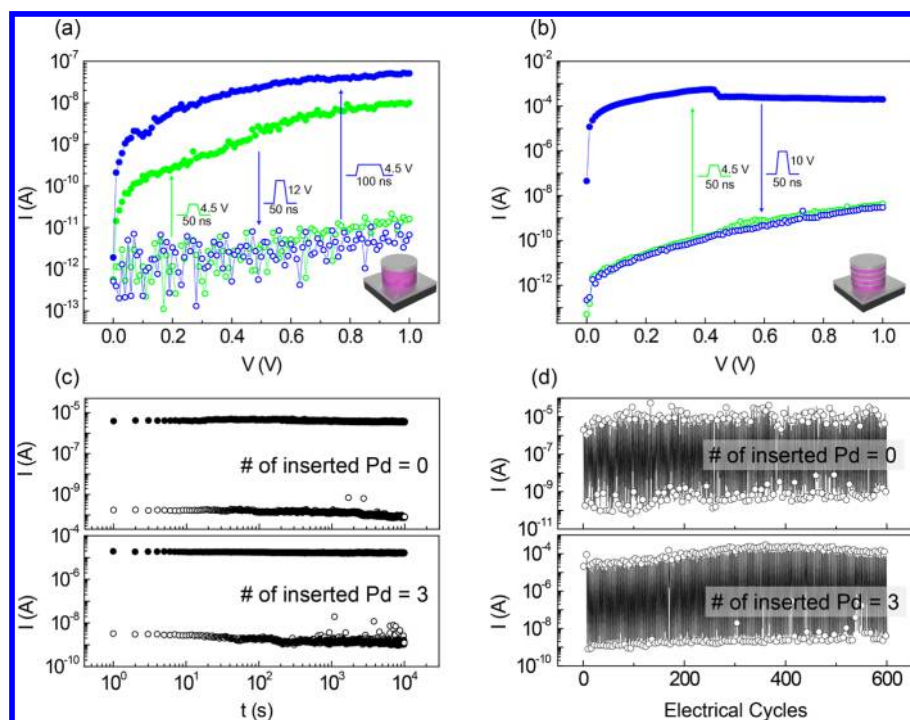


**Figure 3. (a) Switching speed test for a pure $SiO_x$ memory device. (b) Switching speed test for a three-Pd-interlayer $SiO_x$ memory device. The arrows indicate the directions of the ON-state and OFF-state transitions. The rising edge and falling edge of the pulses were 10 ns. (c) Retention test of the selected pure and Pd-interlayer $SiO_x$ memory devices. (d) Pulse endurance cycles of the selected pure (top) and three-Pd-interlayer (bottom) $SiO_x$ memory devices.**

precise switching pulse, a further detailed study is needed based on test structures designed for a ground−signal−ground measurement environment using an ultra-high-resolution pulse generator, a device that we presently do not possess.

Figure 3c,d show the retention and the pulse endurance cycling results for a pure $SiO_x$ memory (number of inserted Pd layers = 0) and a Pd-interlayer $SiO_x$ memory system (number of inserted Pd layers = 3). The switching states of the devices were programmed to be LRS/HRS at a read voltage pulse by applying different voltage pulses for set and reset processes. As shown in Figure 3c, the ON and OFF currents for a pure and a three-Pd-interlayer $SiO_x$ memory device were individually measured at 1.0 V for $10^4$ s with the interval $\Delta t = 1$ s after being set by 5.0 V and reset by 15 V. They all retain the nondestructive switching state with at least a $10^4$ ON/OFF ratio during the $10^4$ s even at high-temperature conditions (Figure S10). Furthermore, they show acceptable endurance properties with at least a $10^4$ ON/OFF ratio during the 600 cycle programming, as shown in Figure 3d. These results demonstrate the competitive switching stability of the Pd-interlayer $SiO_x$ memory device. The Pd-interlayer $SiO_x$ memory can be operated in the bipolar switching mode (Figure S11).

One possible mechanism for our observations is that the inserted Pd layers aid in the formation of the conducting paths at weaker edge regions of each $SiO_x$ layer, leading to the lower $V_{forming}$ than that in a pure $SiO_x$ memory. If the conducting paths were individually formed in the weakest regions of the $SiO_x$ layers and other channels of the $SiO_x$ layers experienced a hard breakdown after the initial electroforming process, there is a possibility that the switching channels would become more sensitive to the applied voltage and become more conducting. In fact, it was observed that each 30 nm $SiO_x$ layer in a Pd/$SiO_x$-Pt-$SiO_x$/Pd memory device can show different breakdown results after the electroforming process. For example, one of the $SiO_x$ layers experiences a hard breakdown that causes low junction resistance due to an electrical short-circuit formation, but the other $SiO_x$ layer experiences a soft breakdown that causes switching behavior (Figure S12). The oxide degradation for thinner oxides at relatively lower voltages can be defined as a soft breakdown;[45] the soft breakdown conduction is non-ohmic and retains insulating properties other than at the conducting Si-filament. Therefore, the inserted conducting Pd layer could lead to lower junction resistance and lower $V_{th}$ as well as a faster switching speed. Another possible mechanism is that the inserted Pd metal could be slightly diffused at the edge of $SiO_x$ layers during the electroforming process and could act as an additional conducting component with the Si, leading to lower resistance of the switching channel. However, we have no direct evidence for this conjecture.

The Pd-interlayer $SiO_x$ memory was also fabricated and characterized on a polyimide (PI) flexible substrate.



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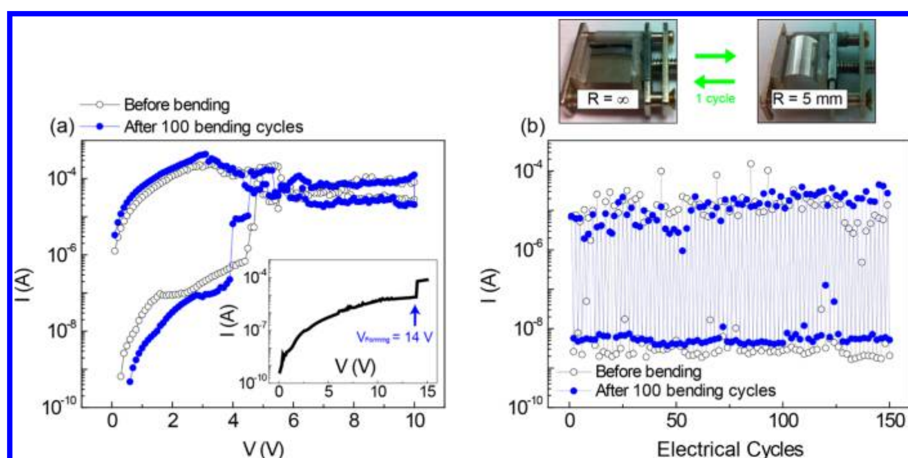


**Figure 4. (a) I−V characteristics for a one-Pd-interlayer $SiO_x$ memory before and after bending (100 times) at $R$ = 5 mm. The inset shows the initial $I-V$ curve for the electroforming process. (b) Pulse endurance cycles of the selected one-Pd-interlayer $SiO_x$ memory device. The top panel shows an example of 1 cycle during the tests. All devices are subjected to similar bending strains, and the measured devices were near the middle of the sample.**

The flexible device fabrication was similar to that used for the rigid device since it involves a low-temperature process (Figure S1). Figure 4a shows the switching $I-V$ curves of the one-Pd-interlayer $SiO_x$ memory devices before bending (defined as the bending radius $R = \infty$) and after repeated bending cycles (100 times) at $R$ = 5 mm. The $V_{forming}$ of the flexible device was found to be ~14 V (the inset of Figure 4a), which demonstrates the substrate-independent $V_{forming}$. Also, the switching $I-V$ curve after 100 bending cycles was similar to that of the flexible device in the flat condition. As shown in Figure 4b, the ON/OFF ratios of flexible devices under different bending cycling conditions (*i.e.*, flat and 100 bending cycles) were maintained at ~$10^3$ during 150 pulse cycles. These results show that the Pd-interlayer $SiO_x$ memory can be fabricated on a flexible substrate at room temperature, and it shows low $V_{forming}$ and good switching stability under mechanical bending conditions. This result offers a simple fabrication method for flexible $SiO_x$ memory devices that have low $V_{forming}$ without any significant degradation of the flexible device.

To better understand the physics behind the reduction of $V_{forming}$ in the Pd-interlayer $SiO_x$ memory device, we employed the probability ($P_b$) of the bond breakdown of the dielectric material that accounts for both the temperature and the electric field.[22,32,33,46] The bond-breaking $P_b$ in the presence of a temperature ($T$) and an electric field ($E$) can be expressed as shown in eq 1:

$$P_b \propto \exp\left(-\frac{\Delta H}{k_B T}\right) \quad (1)$$

$$\Delta H = \Delta H_o - p_o\left(\frac{2+\varepsilon_r}{3}\right)E$$

where $\Delta H$ is the activation energy for bond breakage, $\Delta H_o$ is the activation energy for bond breakage in the absence of $E$ ($\Delta H_o$ = 1 eV for $SiO_2$),[33,47] $p_o$ is the dipole moment of molecular bond ($p_o$ = 3.4 for $SiO_2$),[33] $\varepsilon_r$ is the dielectric constant ($\varepsilon_r$ = 3.9 for $SiO_2$),[33] and $k_B$ is the Boltzmann constant. In fact, the bond breakdown can occur when the $\Delta H \rightarrow 0$ at a certain electric field $E = E_b$. For the case of ideal $SiO_2$, the $E_b$ is calculated to be 15 MV/cm.[33] However, in our pure $SiO_x$ memory junction we have used $E_b = V_{forming}/d$ ($d$ is defined as the thickness of $SiO_x$) ≅ 3.52 MV/cm, which is much lower than the theoretical value due to the formation of conducting paths in weak edge regions and the relative strong polarity of $SiO_x$ due to oxygen vacancies when compared to ideal $SiO_2$. Thus, we can assume that the bond-breaking probability $P_b$ is 1 at $E$ = 3.52 MV/cm in the case of our $SiO_x$ material. Based on the normalization of $P_b$ by $SiO_x$, the bond-breaking $P_b$ for $SiO_x$ can be expressed as in eq 2:

$$P_{b(\text{for } SiO_x)} = \frac{1}{2.56 \times 10^{-13}} \exp\left(-\frac{\Delta H}{k_B T}\right) \quad (2)$$

where $2.56 \times 10^{-13}$ is the normalization factor, which corresponds to $P_b$ = 1 at $E$ = 3.52 MV/cm. From eq 2, we calculate $P_b$ for $SiO_x$ according to the applied voltage, $V$, and the thickness of $SiO_x$, $d$, at room temperature (300 K), as shown in the contour plot in Figure 5a. In Figure 5a, the diagonal dotted line indicates a $P_b$ = 1, which corresponds to the $V_{forming}$ at a given thickness of $SiO_x$. The $V_{forming}$ for different thicknesses of $SiO_x$ (30 and 40 nm) was found to be ~10.5 V and ~14.5 V, respectively, which are similar to the estimated values in Figure 5a (Figures S12 and S13). However, at that scale, the $SiO_x$ devices frequently resulted in a hard breakdown. The 30 nm $SiO_x$ devices that we fabricated showed 100% electrical shorts after a few voltage sweeps (Figure S15). We speculate that this might be due to the relatively short conducting path that has little chance to change the Si NCs into amorphous Si due to its low resistance. It is also unlikely that there is

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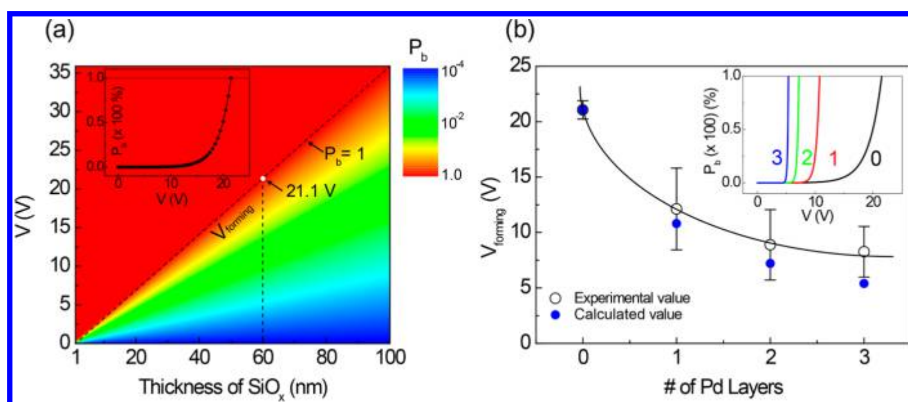


**Figure 5. (a) Contour plots of the calculated data of normalized bond-breaking probability $P_b$ as a function of the thickness of $SiO_x$ under applied voltages. The dotted $V_{Forming}$ line corresponds to $P_b$ = 1. The inset shows the $P_b-V$ curve for a pure $SiO_x$ memory device. (b) Plot of experimental and calculated $V_{Forming}$ as a function of the number of Pd layers. The inset shows the $P_b-V$ curves for zero, one, two, and three Pd interlayers in the $SiO_x$ memory devices.**

further aggregation of the Si NCs in the path after repeated voltage sweeps. Therefore, the conducting-interlayer $SiO_x$ memory system can be distinguished from just reducing the $SiO_x$ thickness in terms of the stable switching performance, even though they have similar $V_{forming}$.

In order to estimate the $V_{forming}$ for the Pd-interlayer $SiO_x$ memory device, we assumed that the conducting paths at each $SiO_x$ layer are not produced at the same time. In other words, one of the conducting paths that is located on the top or bottom $SiO_x$ layer was completely formed prior to other paths, which is dependent on the bias polarity of the initial electroforming process. It was previously reported that the conductive nanofilament in metal oxide and $SiO_x$ films generates excesses of vacancies near the anode during the electroforming process.[48,49] From this assumption, the bond-breaking probability $P_b$ for Pd-interlayer $SiO_x$ can be expressed based on the multiplication of individual $P_b$ for each $SiO_x$ intermediate layer as in eq 3:

$$P_{b(\text{for Pd-interlayer SiO}_x)} = \prod_1^n P_b{}^n = \prod_1^n \frac{1}{2.56 \times 10^{-13}} \exp\left(-\frac{\Delta H^n}{k_B T}\right) \tag{3}$$

where $n$ is the number of $SiO_x$ layers in a junction. The degrees of weaknesses in $SiO_x$ are not considered in this equation. The inset in Figure 5b shows the $P_b$ for Pd-interlayer $SiO_x$ memory devices, which can indicate the $V_{forming}$ corresponding to each $P_b$ = 1. Figure 5b shows the experimental and the calculated $V_{forming}$ for Pd-interlayer $SiO_x$ memory devices according to the number of inserted Pd layers, which are in good agreement. They both show a similar trend; the difference of $V_{forming}$ in the different number of Pd-interlayer $SiO_x$ memory devices becomes close when the number of inserted Pd layers was increased.

## CONCLUSIONS

In summary, we report the fabrication of conducting-interlayer $SiO_x$ nonvolatile memory devices using Pd, Ti, carbon, or MLG at room temperature. When compared to a pure $SiO_x$ memory device, the Pd-interlayer $SiO_x$ memory device was shown to provide performance advantages including low $V_{forming}$ (~8.3 V), low $V_{th}$ (~3.7 V), and fast switching speed (≤50 ns) for complete set processes, while maintaining the ON−OFF ratio and endurance of pure $SiO_x$ memories. In addition, we have demonstrated that the Pd-interlayer $SiO_x$ flexible memory device also shows low $V_{forming}$ and stable switching even after 100 bending cycles. The reduction of the $V_{forming}$ in the Pd-interlayer $SiO_x$ memory junction is well-explained by the normalized bond-breaking probability when considering the applied voltage and the thickness of the $SiO_x$ layer. The Pd-interlayer $SiO_x$ memory system has promise to satisfy the prerequisite conditions for future nonvolatile memory applications in terms of the enhancement of the switching properties and low-temperature fabrication accessibility.

## MATERIALS AND METHODS.

**Pd-, Ti-, or Carbon-Interlayer $SiO_x$ Memory Device.** The memory cells are fabricated on p-type (100) Si wafers (1.5 cm × 1.5 cm) covered with thermally grown 300-nm-thick $SiO_2$ and on a 150-μm-thick polyimide plastic substrate (McMaster-CARR). There are no significant differences between the fabrication processes for the rigid and flexible $SiO_x$ memory due to the low-temperature process. First, a Pt (20 nm) bottom electrode was deposited on the substrate by sputtering after a typical cleaning process with acetone, isopropyl alcohol, and deionized water by ultrasonication for 3 min. Then, photoresist (MICROPOSIT S1813) was spin-coated on the samples, and patterning was done using a positive photomask for making the cells. The radii of the cells were 25 and 50 μm. The active

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memory materials were then fabricated on top of the Pt bottom electrode by depositing patterned Pd (40 nm)/$SiO_x$ (30 nm)/Pd (or Ti) (5 nm)/$SiO_x$ (30 nm) by electron beam evaporation at a pressure of $\sim 10^{-6}$ Torr and a deposition rate of ~0.5 to 1.0 Å/s at room temperature. The carbon (5 nm) interlayer was deposited by sputtering. After the liftoff process to remove the nonactive regions, the memory cell was formed (Figure S1a–c).

**MLG-Interlayer $SiO_x$ Memory Device.** We prepared multilayer graphene films by chemical vapor deposition using $H_2$ and $CH_4$ at 1000 °C,[50,51] as shown in the SEM and TEM images for MLG (Figures S2d,e). After the deposition of $SiO_x$(30 nm)/Pt (20 nm) on the substrate, the MLG was transferred to the sample (Figure S2a). The samples were then thermally annealed in a furnace at 350 °C under Ar (500 sccm) and $H_2$ (50 sccm) for 20 min at a pressure of ~8 Torr in order to make good adhesion between the MLG and the first layer of $SiO_x$. The annealing process could affect the electroforming process.[23,32] After making the pattern on top of the MLG by photolithography, the Pd (40 nm)/$SiO_x$ (30 nm) was deposited on the top of the MLG by electron beam evaporation. After the liftoff process for removing the nonactive region, a reactive-ion etching process was performed to remove the exposed MLG/$SiO_x$ layer (Figure S2b,c).

*Conflict of Interest:* The authors declare the following competing financial interest(s): Rice University owns several patents and patent applications for $SiO_x$ memories.

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*Supporting Information Available:* Additional methods and figures. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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