NANO LETTERS

Letter

pubs.acs.org/NanoLett

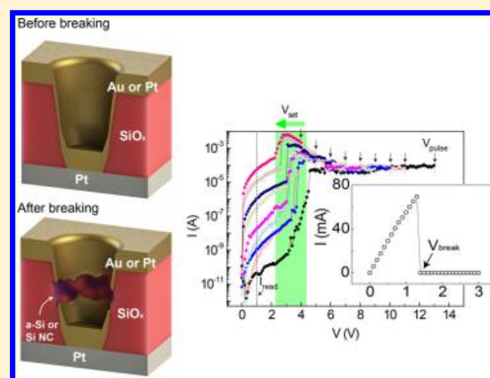
# Nanoporous Silicon Oxide Memory

Gunuk Wang,[†,‡] Yang Yang,[†,‡] Jae-Hwang Lee,[§] Vera Abramova,[†] Huilong Fei,[†] Gedeng Ruan,[†] Edwin L. Thomas,[†,‡,§] and James M. Tour*[,†,‡,§,∥]

[†]Department of Chemistry, [‡]Smalley Institute for Nanoscale Science and Technology, [§]Department of Materials Science and NanoEngineering, and [∥]Department of Computer Science, Rice University, 6100 Main Street, Houston, Texas 77005, United States

*Supporting Information*

**ABSTRACT:** Oxide-based two-terminal resistive random access memory (RRAM) is considered one of the most promising candidates for next-generation nonvolatile memory. We introduce here a new RRAM memory structure employing a nanoporous (NP) silicon oxide ($SiO_x$) material which enables unipolar switching through its internal vertical nanogap. Through the control of the stochastic filament formation at low voltage, the NP $SiO_x$ memory exhibited an extremely low electroforming voltage (~1.6 V) and outstanding performance metrics. These include multibit storage ability (up to 9-bits), a high ON−OFF ratio (up to $10^7$ A), a long high-temperature lifetime ($\geq 10^4$ s at 100 °C), excellent cycling endurance ($\geq 10^5$), sub-50 ns switching speeds, and low power consumption (~$6 \times 10^{-5}$ W/bit). Also provided is the room temperature processability for versatile fabrication without any compliance current being needed during electroforming or switching operations. Taken together, these metrics in NP $SiO_x$ RRAM provide a route toward easily accessed nonvolatile memory applications.




**KEYWORDS:** *Nanoporous, silicon oxide, nonvolatile memory, resistive memory, $SiO_x$*

Downloaded by UNIV OF MASSACHUSETTS AMHERST on September 14, 2015 | http://pubs.acs.org
Publication Date (Web): July 8, 2014 | doi: 10.1021/nl501803s

For more than a half century, conventional Si-based complementary metal−oxide−semiconductor (CMOS) transistors have been the mainstay of the electronic memory industry. Furthermore, Si-based flash memory's superior performance and its ease of fabrication compared to competing memory technologies has made it the dominant form of CMOS memory.[1−3] However, the high standards of next-generation memory driven by rapidly growing demands have revealed the limits of current Si-based flash memory technology in terms of its fundamental scaling limitations, energy consumption, cost, and few microsecond switching speed.[4−6] Although a wide variety of oxide-based materials and device structures for the replacement of the Si-based flash memories have been extensively investigated,[7−10] none have adequately addressed future memory projections. Generally, the oxide-based RRAMs can be categorized into unipolar and bipolar memories according to the required electric polarity for the switching.[5,7,9]

Many of the unipolar memories have demonstrated that they are operated by nanoscale filamentary switching which allow them to follow an aggressive scaling trend;[7,11,12] however, nanoscale metallic filaments can exhibit unstable switching behaviors and high or unpredictable forming voltages ($V_{forming}$) due to the difficulty in controlling their stochastic formation.[13−15] In contrast, bipolar memory has comparative advantages in the switching stability by an ionic movement or a redox process, with lower $V_{forming}$, and a broader range of materials availability.[5,8,10,16−19] However, these come at the expense of lower switching ON−OFF ratios, limited thermal stability of the materials, or the limits of integration architectures to suppress sneak-currents in high-density crossbar array.[5,8,10,16−19] Both unipolar and bipolar memory fabrications often involve high-temperature processes for materials depositions.[5,10,11,13−16,18] Moreover, the devices commonly have a high switching current, and they need a compliance current ($I_c$) for preventing an electrical short,[5,7,9,14,17,18] which requires an additional resistor on each cell and increased power consumption. To satisfy all requirements for the future nonvolatile memory, it is therefore preferential to resolve the aforementioned challenges of each oxide-based memory system without any designated $I_c$ or high temperature fabrication process.

Nanoporous (NP) metal oxides have been widely used in electronics for energy production and storage.[20−22] While NP materials have been used as templates for oxide memory applications,[23] they have not yet been used as the active switching medium for resistive nonvolatile memory application.

In this report we introduce a straightforward and simple approach toward a reliable nonvolatile RRAM device using a NP $SiO_x$ (where $1 < x < 2$) structure as a unipolar switching medium. It is a new implementation of a nanoporous material in memory devices with metrics that meet those needed for the industrial performance. These outperform present unipolar memory systems and can also bring advantages to bipolar

**Received:** May 14, 2014
**Revised:** June 16, 2014
**Published:** July 3, 2014

ACS Publications © 2014 American Chemical Society

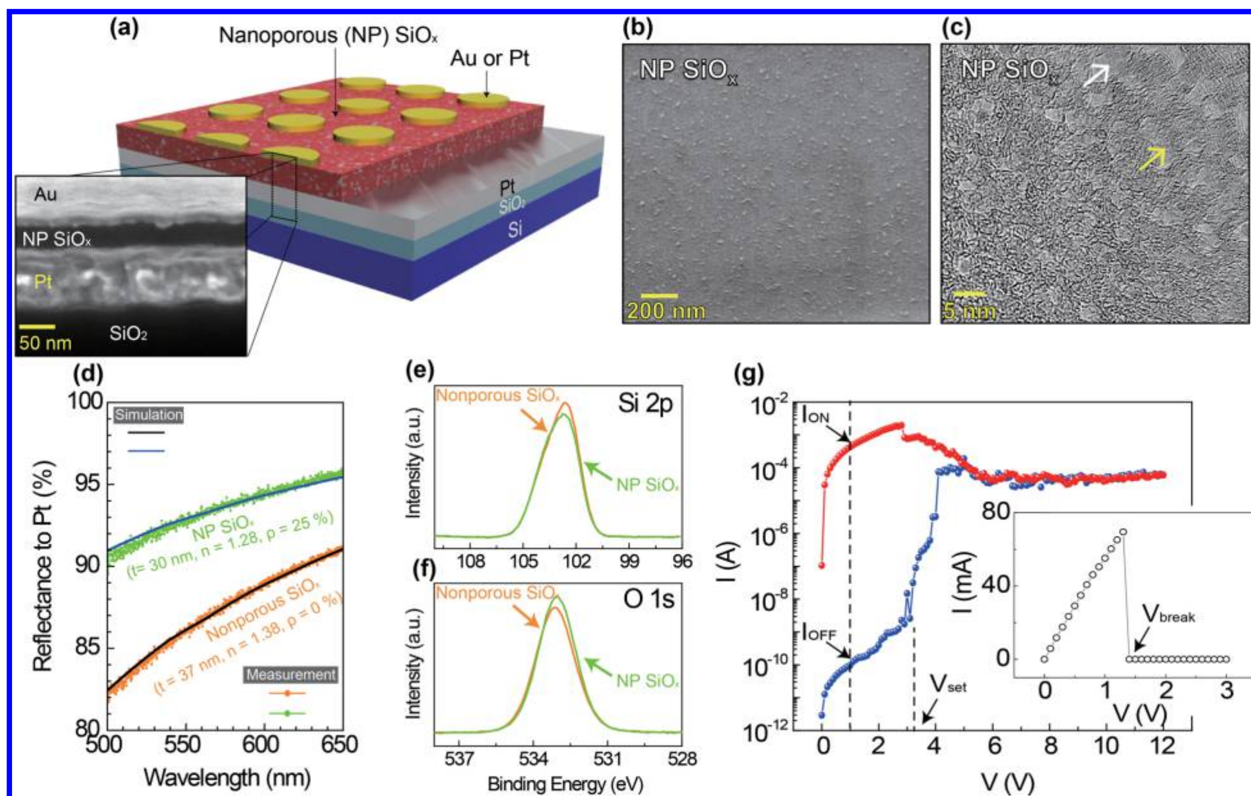



**Figure 1.** (a) Schematic illustration of the NP $SiO_x$ memory device with the cross-sectional SEM image of a selected cell. (b) SEM image of the NP $SiO_x$ film tilted at 45°. (c) TEM image of the NP $SiO_x$ film. The white arrow points to a void, and the yellow arrow points to the amorphous $SiO_x$. See Figure S1 for larger images. (d) The reflectance spectra of nonporous and NP $SiO_x$ layers on a Pt-deposited silicon substrate with the numerical fitting curves based on an analytical formula using the measured thickness. (e and f) XPS Si 2p and O 1s spectra of the nonporous and NP $SiO_x$ films ($x$ = 1.63−1.76), respectively. (g) The representative $I-V$ characteristics of the NP $SiO_x$ with the initial $I-V$ sweep (inset).

memories. Using this NP $SiO_x$ structure, we are able to control the stochastic formation of the switching filament which leads to significant improvements in device metrics, and it can be fabricated at room temperature.

Figure 1a is a schematic diagram of the NP $SiO_x$ memory cells along with a cross-sectional scanning electron microscope (SEM) image at the middle of the cell. The NP $SiO_x$ structure was prepared by anodic galvanostatic etching of $SiO_2$ with 1 vol % HF in ethanol solution to afford a significantly roughened morphology of the deposited $SiO_x$ film (Figure 1b and Figure S1 in the Supporting Information). Transmission electron microscopy (TEM) micrographs show that nanoscale holes in the $SiO_x$ film are approximately randomly distributed with diameters ranging from 2 to 6 nm (Figure 1c and Figure S1). The average porosity of the NP $SiO_x$ film can be defined by its effective refractive index ($n$) based on the Bruggemann effective medium approximation,[24] which was estimated by the numerical fitting of a visible reflectance spectrum of the NP $SiO_x$ film. The optically defined average porosity value of the NP $SiO_x$ material was $\rho$ = 25% (Figure 1d); the etching process created a substantially nanoporous $SiO_x$ material. However, no significant change was made in their composition according to X-ray photoelectron spectroscopy (XPS) of NP $SiO_x$ ($x$ = 1.63−1.76) relative to nonporous $SiO_x$ (Figure 1e−f and Figure S2). Note that the Pt layer is fully exposed by overetching if 5 vol % HF is used (Figure S2). Additional details on the fabrication process, measurements, and porosity calculation for the NP $SiO_x$ memory are provided in the Supporting Information. The top contacts (Au or Pt) were subsequently applied, and no further etching of the individual devices is required (Figure S2).

Figure 1g shows a typical switching $I-V$ curve of the NP $SiO_x$ memory after an electroforming process; no $I_c$ is applied. All NP $SiO_x$ memories showed a unipolar switching behavior similar to that of a nonporous $SiO_x$ memory with $I_{ON}$ and $I_{OFF}$ controlled by a constant polarity of set and reset voltages.[15,19] This is a greatly simplified electroforming process relative to nonporous $SiO_x$ (Figure S3). Electroforming of the NP $SiO_x$ memory can be achieved by a single low-voltage sweep to a breaking voltage ($V_{break}$ = 1.4 V) where a current suddenly drops; thus we can define the $V_{break}$ as the $V_{forming}$, as shown in the inset of Figure 1g. In addition, the junction vertical edge of nonporous $SiO_x$ memory is essential for the electroforming process and switching[15] while not needed for the NP $SiO_x$ (Figure S4), exemplifying the marked ease in fabrication demands. The $I-V$ behavior in Figure 1g inset is typical of metal filament breakage, and at that point, the Si nanofilament is likely formed in the metal gap region.[25] The NP $SiO_x$ memory with a Au top-electrode required $V_{forming}$ of only ~1.6 V on average to form a switching path, compared to the significantly higher $V_{forming}$ for a nonporous $SiO_x$ memory of >20 V (Figure S4).[15] The low forming voltage and a single sweep for the electroforming process are advantageous in high-density integration of nanoscale memory cells with diodes by avoiding potential breakdowns due to the high forming voltage and by repeated voltage sweeps.[15,26] The single low voltage sweep also mitigates the problematic Joule-heating-damage to the surrounding $SiO_x$ material, thus reducing the uncertainty in the stochastic formation of the switching filament. The NP

Downloaded by UNIV OF MASSACHUSETTS AMHERST on September 14, 2015 | http://pubs.acs.org
Publication Date (Web): July 8, 2014 | doi: 10.1021/nl501803s

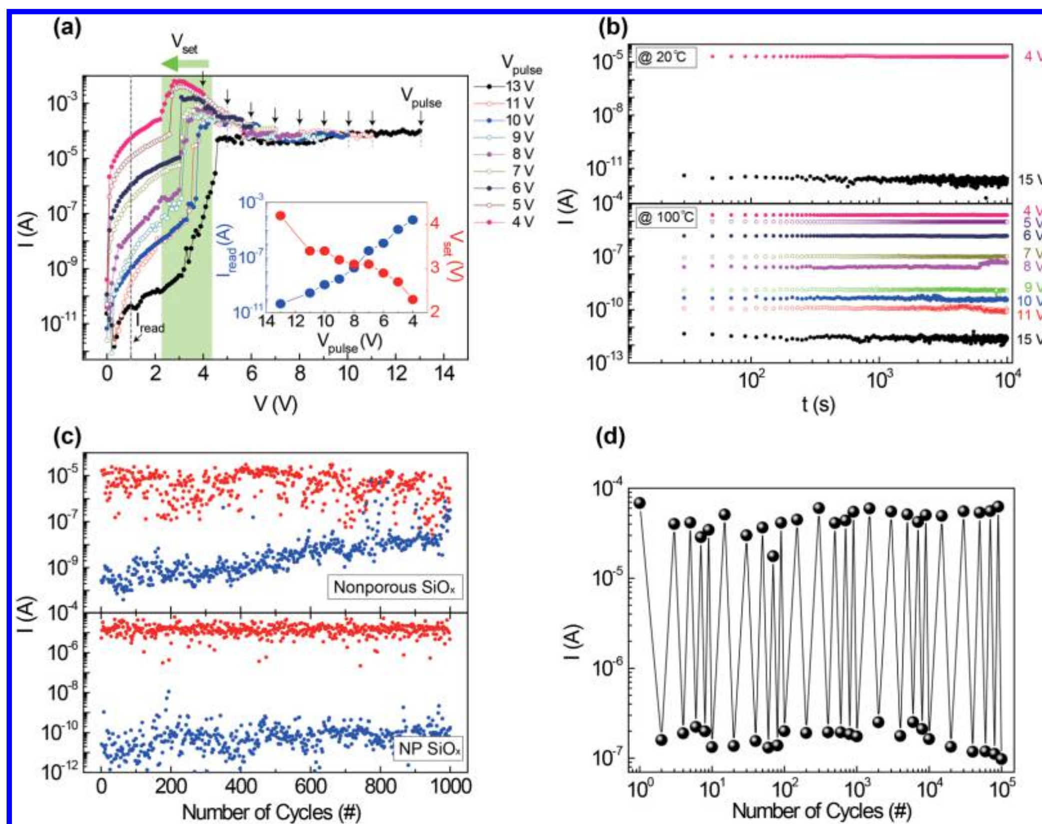



**Figure 2.** (a) A set of $I-V$ characteristics of a single NP $SiO_x$ cell after exposure to different $V_{pulse}$ changed from 13 to 4 V with $\Delta V$ = 1 V. The Au top-contact had a 100 $\mu$m radius, while the NP $SiO_x$ was ~40 nm thick. (b) Retention tests on a NP $SiO_x$ cell after different $V_{pulse}$ processes during $10^4$ s at 20 (top) and 100 °C (bottom). (c) Endurance cycling test of a representative nonporous and NP $SiO_x$ cell for $10^3$ cycles. (d) Endurance cycling test of the NP $SiO_x$ cell for $10^5$ cycles. The set voltage = 5 V, reset voltage = 15 V, and read voltage = 1 V (~500 $\mu$s for set, reset, and read voltage pulses).

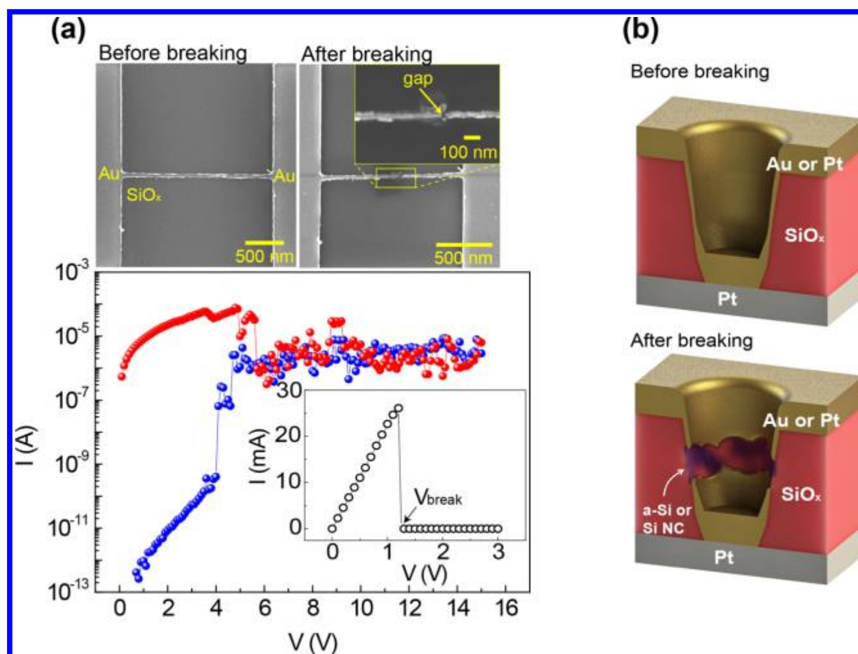



**Figure 3.** (a) Top SEM images show the planar Au/$SiO_x$ memory device before (left) and after (right) the breakdown of the Au nanowire with the enlarged via in the inset. The bottom plot shows typical $I-V$ switching characteristics of a nanogap device with a Au nanowire width of 60 nm (top figures) with the initial $I-V$ sweep (Inset). (b) The schematics of the NP $SiO_x$ memory structure before (top) and after (bottom) the breakdown of Au (or Pt) channel though a nanohole.

Downloaded by UNIV OF MASSACHUSETTS AMHERST on September 14, 2015 | http://pubs.acs.org
Publication Date (Web): July 8, 2014 | doi: 10.1021/nl501803s

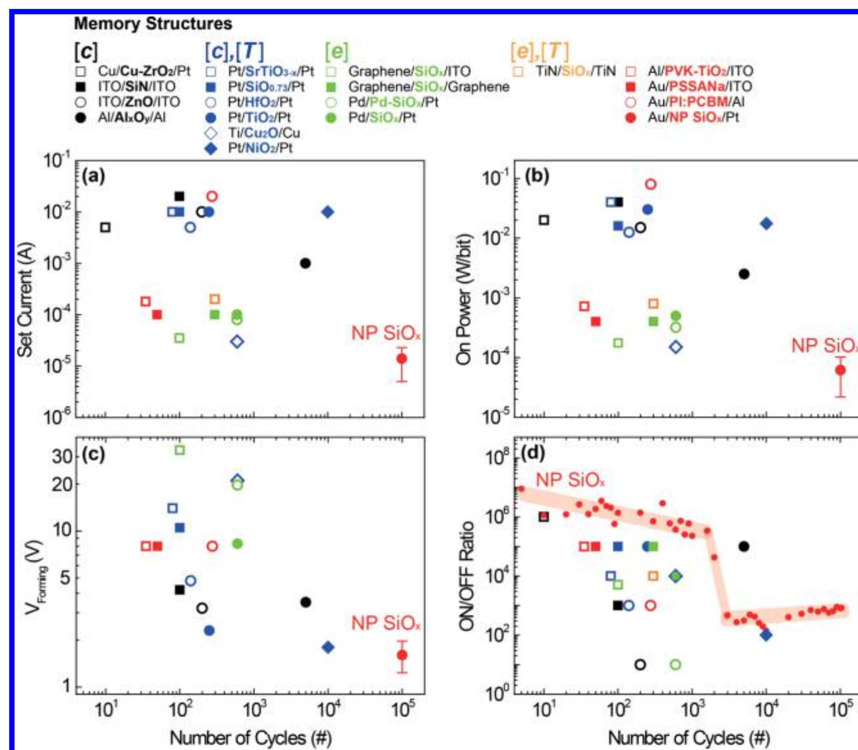



**Figure 4.** (a) Set current, (b) ON power, (c) $V_{forming}$, and (d) ON−OFF ratio corresponding to the number of endurance cycles for the NP $SiO_x$ and other reported unipolar memory devices. The notations of [c], [e], or [T] indicate that the $I_c$, the junction vertical edge, and a high temperature process are necessary for switching behavior for the respective devices. Depending on the requirements of the memory switching, the different colors are expressed. The unipolar memory structures using doped Si electrodes are excluded because of the difficulty of three-dimensional stackable memories for this route and also the high thermal budget required.

$SiO_x$ memory using instead a Pt top-electrode shows similar switching behavior with, as expected, a slightly higher $V_{forming} \cong 2.1$ V (Figure S5). We found that similar switching speeds (sub-50 ns, measurement limit) for the set and reset process were observed in the NP $SiO_x$ memory (Figure S6) as compared to that of the nonporous $SiO_x$ memory.[27]

To evaluate the sensitivity and stability of the switching filament in the NP $SiO_x$ memory, we tested the switching current levels and the retentions at 1.0 V after different voltage pulses ($V_{pulse}$) on the same cell of the device. Figure 2a shows the switching $I$−$V$ behavior for 9-bits after different $V_{pulse}$ changed from 13 to 4 V (with $\Delta V = 1$ V). Figure 2b shows retention results at two different temperatures after the $V_{pulse}$. The ON−OFF ratios of each state are varied from ∼2.5 to $\sim 10^7$ according to the $V_{pulse}$ and are maintained for $10^4$ s even at 100 °C. When the $V_{pulse}$ was decreased, the read-current ($I_{read}$) at 1.0 V increased while the set voltage ($V_{set}$) decreased, similar to the behavior of the nonporous $SiO_x$ memory.[15,28] It has been suggested that the conducting filament consisting of silicon nanocrystals (Si NCs) can be significantly disrupted by the higher $V_{pulse}$, which results in lower $I_{read}$.[19,28] To our knowledge, however, this is the first demonstration of an oxide-based memory device with a 9-bits switching ability with ON-OFF ratio $\cong 10^7$ A, making this device promising as a multibit memory system. Moreover, this multibit feature, coupled with the 5 nm diameter Si NC filament,[25] makes the RRAM device attractive for aggressive equivalent scaling.

The switching endurance stability is a crucial factor for the practical application of nonvolatile memory devices, which is one of the main challenges in unipolar memory.[13−15,25] In the case of nonporous $SiO_x$, the ON- and OFF-current values became similar after $10^3$ cycles due to the extensive aggregation of the Si NCs formed in the switching path by accumulated voltage stresses,[25] which causes the indistinctive switching states (Figure 2c top). In contrast, the ON−OFF ratio of the NP $SiO_x$ memory was significantly less degraded during $10^3$ cycles and shows at least $\sim 10^6$ ON−OFF ratio (Figure 2c bottom). Interestingly at $\sim 2 \times 10^3$ cycles, the OFF-current increased and was maintained $\sim 10^{-7}$ A (Figure S7). After that event, an excellent endurance property of $\sim 10^3$ ON−OFF ratio during $10^5$ cycles was observed, as shown in Figure 2d (see also full data set in Figure S7).

To identify the switching mechanism of the NP $SiO_x$ memory, we fabricated a planar model structure of the $SiO_x$ memory device using an Au nanowire with a width of 60 nm (see Supporting Information). When an initial voltage sweep was applied to the Au nanowire, an electrical breakdown occurred at 1.25 V by the electromigration of Au, and the electrical current suddenly dropped (top and inset of Figure 3a), which would be conceptually similar to the occurrence in the vertical NP $SiO_x$ memory. The SEM image shows a relatively dark region near the gap indicating the intrinsic postbreakdown of underlying $SiO_x$ by the thermal damage induced by electromigration (Figure S8).[25] A subsequent electric potential (>1.25 V) at the local confinement (≤20 nm) could easily change the $SiO_x$ to a Si-phase (Si NC or a-Si), as we demonstrated previously.[25] The planar model device showed the typical $SiO_x$ unipolar switching behavior after this breakdown process (Figure 3a), which offers a route to decrease the $V_{forming}$ without a thermal annealing treatment. The postbreakdown process of $SiO_x$ could help to form the switching filament at a low bias, which leads to the extended

Downloaded by UNIV OF MASSACHUSETTS AMHERST on September 14, 2015 | http://pubs.acs.org
Publication Date (Web): July 8, 2014 | doi: 10.1021/nl501803s

endurance cycles as well (Figure S8). Note that we previously reported $SiO_x$ memories analogous to this planar model structure but with various electrode materials including α-carbon, TiN, carbon nanotubes, and graphene, and they all showed a similar breakdown process at an initial $I-V$ sweep.[25,27,29,30] Therefore, we suggest that the switching mechanism of the NP $SiO_x$ can be understood by the breakdown process of Au on the sidewalls of nanoholes through the $SiO_x$ film as illustrated in Figure 3b. Interestingly, the initial switching state of the NP $SiO_x$ memory has either an ON or OFF state after the breakdown process, which means that the switching path in the vertical-nanogap is mainly formed by a Si NC or a-Si (Figure S4).[25] This mechanism, based on the electromigration of a metal wire, can also explain why the $V_{forming}$ of NP $SiO_x$ using the more refractory Pt top-electrode has a slightly higher value than that of the NP $SiO_x$ using the Au top-electrode (Figures S4 and S5).

The demonstrated RRAM switching parameters of the NP $SiO_x$ memory, including the set current, the ON power, the $V_{forming}$, and ON−OFF ratio with the endurance cycles, are compared with the reported unipolar memories as well as other types of nonporous $SiO_x$ memories using metal electrodes, as shown in Figure 4. In the comparison, the set-current ($1.4 \pm 0.9 \times 10^{-5}$ A), the ON power ($6.2 \pm 4.0 \times 10^{-5}$ W/bit), and $V_{forming}$ ($1.6 \pm 0.4$ V) are the lowest values, while the ON−OFF ratio was slightly higher at the given number of cycles for this NP $SiO_x$ memory (see table in the Supporting Information).[31] Importantly, many unipolar memories require $I_c$ (denoted as "[$c$]" in Figure 4), junction edge-switching [$e$], or high temperature processing [$T$] for the switching, whereas the NP $SiO_x$ devices do not require any of these; an important consideration for large-scale fabrication of nonvolatile memory technologies.

In summary, the RRAM memory structure using a NP $SiO_x$ can show excellent switching behavior far beyond the current unipolar memory systems and enables simpler fabrication and operating procedures than bipolar RRAMs. The switching mechanism can be explained by the breakdown process of an initial metal connection at a low bias regime that can effectively mitigate the undesired Joule-heating-damage of the switching path at $V_{forming}$. Our results suggest that the NP $SiO_x$ memory system could offer a new device paradigm for future memory applications.

## ■ ASSOCIATED CONTENT

### Supporting Information

Device fabrication details, electroforming process, endurance cycles and comparison of switching parameters for other unipolar memory. This material is available free of charge via the Internet at http://pubs.acs.org.

## ■ AUTHOR INFORMATION

### Corresponding Author

*E-mail: tour@rice.edu.

### Author Contributions

G.W. and Y.Y. contributed equally to this work. G.W. designed and performed the experiments and wrote the manuscript. G.W. and Y.Y. fabricated the devices. Y.Y., J.-H.L., V.A., H.F., and G.R. assisted in measurements. G.W., Y.Y., J.-H.L., and J.M.T. analyzed and interpreted the data and wrote the manuscript. E.L.T contributed to discussions regarding the SEM, TEM, and optical studies. J.M.T. planned and supervised all phases of the project and corrected the manuscript. All authors proofed the manuscript.

### Notes

The authors declare no competing financial interest.

## ■ REFERENCES

(1) Bez, R.; Camerlenghi, E.; Modelli, A.; Visconti, A. Introduction to Flash Memory. *Proc. IEEE* **2003**, *91*, 489−502.
(2) Lankhorst, M. H. R.; Ketelaars, B. W. S. M. M.; Wolters, R. A. M. Low-Cost and Nanoscale Non-Volatile Memory Concept for Future Silicon Chips. *Nat. Mater.* **2005**, *4* (4), 347−352.
(3) Thompson, S. E.; Chau, R. S.; Ghani, T.; Mistry, K.; Tyagi, S.; Bohr, M. T. In Search of "Forever," Continued Transistor Scaling One New Material at a Time. *IEEE Trans. Semiconduct. Mater.* **2005**, *18*, 26−36.
(4) *International Technology Roadmap for Semiconductors*: ITRS 2013 Edition-Emerging Research Devices; http://www.itrs.net/Links/2013ITRS/Home2013.htm.
(5) Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-Based Resistive Switching Memories−Nanoionic Mechanisms, Prospects, and Challenges. *Adv. Mater.* **2009**, *21*, 2632−2663.
(6) Hamann, H. F.; O'Boyle, M.; Martin, Y. C.; Rooks, M.; Wickramasinghe, H. K. Ultra-High-Density Phase-Change Storage and Memory. *Nat. Mater.* **2006**, *5*, 383−387.
(7) Sawa, A. Resistive Switching in Transition Metal Oxides. *Mater. Today* **2008**, *11*, 28−36.
(8) Yang, J. J.; Strukov, D. B.; Stewart, D. R. Memristive Devices for Computing. *Nat. Nanotechnol.* **2013**, *8*, 13−24.
(9) Waser, R.; Aono, M. Nanoionics-Based Resistive Switching Memories. *Nat. Mater.* **2007**, *6*, 833−840.
(10) Lee, M.-J.; Lee, C. B.; Lee, D.; Lee, S. R.; Chang, M.; Hur, J. H.; Kim, Y.-B.; Kim, C.-J.; Seo, D. H.; Seo, S.; Chung, U. I.; Yoo, I.-K.; Kim, K. A Fast, High-Endurance and Scalable Non-Volatile Memory Device Made from Asymmetric $Ta_2O_{5-x}/TaO_{2-x}$ Bilayer Structures. *Nat. Mater.* **2011**, *10*, 625−630.
(11) Kim, K. M.; Jeong, D. S.; Hwang, C. S. Nanofilamentary Resistive Switching in Binary Oxide System; a Review on the Present Status and Outlook. *Nanotechnology* **2011**, *22*, 254002.
(12) Chen, J.-Y.; Hsin, C.-L.; Huang, C.-W.; Chiu, C.-H.; Huang, Y.-T.; Lin, S.-J.; Wu, W.-W.; Chen, L.-J. Dynamic Evolution of Conducting Nanofilament in Resistive Switching Memories. *Nano Lett.* **2013**, *13*, 3671−3677.
(13) Lee, W.; Park, J.; Kim, S.; Woo, J.; Shin, J.; Choi, G.; Park, S.; Lee, D.; Cha, E.; Lee, B. H.; Hwang, H. High Current Density and Nonlinearity Combination of Selection Device Based on $TaO_x/TiO_2/TaO_x$ Structure for One Selector−One Resistor Arrays. *ACS Nano* **2012**, *6*, 8166−8172.
(14) Kim, G. H.; Lee, J. H.; Ahn, Y.; Jeon, W.; Song, S. J.; Seok, J. Y.; Yoon, J. H.; Yoon, K. J.; Park, T. J.; Hwang, C. S. 32 × 32 Crossbar Array Resistive Memory Composed of a Stacked Schottky Diode and Unipolar Resistive Memory. *Adv. Funct. Mater.* **2013**, *23*, 1440−1449.
(15) Wang, G.; Raji, A.-R. O.; Lee, J.-H.; Tour, J. M. Conducting-Interlayer $SiO_x$ Memory Devices on Rigid and Flexible Substrates. *ACS Nano* **2014**, *8*, 1410−1418.
(16) Yoshida, C.; Kinoshita, K.; Yamasaki, T.; Sugiyama, Y. Direct Observation of Oxygen Movement During Resistance Switching in NiO/Pt Film. *Appl. Phys. Lett.* **2008**, *93*, 042106.
(17) Choi, B. J.; Torrezan, A. C.; Norris, K. J.; Miao, F.; Strachan, J. P.; Zhang, M.-X.; Ohlberg, D. A. A.; Kobayashi, N. P.; Yang, J. J.; Williams, R. S. Electrical Performance and Scalability of Pt Dispersed $SiO_2$ Nanometallic Resistance Switch. *Nano Lett.* **2013**, *13*, 3213−3217.
(18) Yang, Y.; Choi, S.; Lu, W. Oxide Heterostructure Resistive Memory. *Nano Lett.* **2013**, *13*, 2908−2915.
(19) Wang, G.; Lauchner, A. C.; Lin, J.; Natelson, D.; Palem, K. V.; Tour, J. M. High-Performance and Low-Power Rewritable $SiO_x$ 1 kbit One Diode−One Resistor Crossbar Memory Array. *Adv. Mater.* **2013**, *25*, 4789−4793.

Downloaded by UNIV OF MASSACHUSETTS AMHERST on September 14, 2015 | http://pubs.acs.org
Publication Date (Web): July 8, 2014 | doi: 10.1021/nl501803s

(20) Ryan, J. V.; Berry, A. D.; Anderson, M. L.; Long, J. W.; Stroud, R. M.; Cepak, V. M.; Browning, V. M.; Rolison, D. R.; Merzbacher, C. I. Electronic Connection to the Interior of a Mesoporous Insulator with Nanowires of Crystalline $RuO_2$. *Nature* **2000**, *406*, 169−172.
(21) Lee, M. M.; Teuscher, J.; Miyasaka, T.; Murakami, T. N.; Snaith, N. J. Efficient Hybrid Solar Cells Based on Meso-Superstructured Organometal Halide Perovskites. *Science* **2012**, *338*, 643−647.
(22) Brezesinski, T.; Wang, J.; Tolbert, S. H.; Dunn, B. Ordered Mesoporous $\alpha$-$MoO_3$ with Iso-Oriented Nanocrystalline Walls for Thin-Film Pseudocapacitors. *Nat. Mater.* **2010**, *9*, 146−151.
(23) Hong, S.; Choi, T.; Jeon, J. H.; Kim, Y.; Lee, H.; Joo, H.-Y.; Hwang, I.; Kim, J.-S.; Kang, S.-O.; Kalinin, S. V.; Park, B. H. Large Resistive Switching in Ferroelectric $BiFeO_3$ Nano-Island Based Switchable Diodes. *Adv. Mater.* **2013**, *25*, 2339−2343.
(24) Ho, P. K. H.; Stephen, D.; Thomas; Friend, R. H.; Tessler, N. All-Polymer Optoelectronic Devices. *Science* **1999**, *285*, 233−236.
(25) Yao, J.; Zhong, L.; Natelson, D.; Tour, J. M. In Situ Imaging of the Conducting Filament in a Silicon Oxide Resistive Switch. *Sci. Rep.* **2012**, *2*, 242.
(26) Sze, S. M.; Kwok, K. N. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley & Sons: New York, 2007.
(27) Yao, J.; Lin, J.; Dai, Y.; Ruan, G.; Yan, Z.; Li, L.; Zhong, L.; Natelson, D.; Tour, J. M. Highly Transparent Nonvolatile Resistive Memory Devices from Silicon Oxide and Graphene. *Nat. Commun.* **2012**, *3*, 1101.
(28) Yao, J.; Zhong, L.; Natelson, D.; Tour, J. Intrinsic Resistive Switching and Memory Effects in Silicon Oxide. *Appl. Phys. A: Mater. Sci. Process.* **2011**, *102*, 835−839.
(29) Yao, J.; Zhong, L.; Zhang, Z.; He, T.; Jin, Z.; Wheeler, P. J.; Natelson, D.; Tour, J. M. Resistive Switching in Nanogap Systems on $SiO_2$ Substrates. *Small* **2009**, *5*, 2910−2915.
(30) He, C.; Shi, Z.; Zhang, L.; Yang, W.; Yang, R.; Shi, D.; Zhang, G. Multilevel Resistive Switching in Planar Graphene/$SiO_2$ Nanogap Structures. *ACS Nano* **2012**, *6*, 4214−4221.
(31) The switching parameters from literature are summarized in the Supporting Information (Table S1).

Downloaded by UNIV OF MASSACHUSETTS AMHERST on September 14, 2015 | http://pubs.acs.org
Publication Date (Web): July 8, 2014 | doi: 10.1021/nl501803s