

Design and Prototyping of MWPC Preamp Electronics
for Use in the Charged Pion Polarizability Experiment
at Jefferson Lab

A Senior Honors Thesis Presented

By

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Approved

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1 Introduction

Nuclear phenomena occur on a scale which makes them impossible to observe directly. As a result, sophisticated detector systems and computer algorithms must be used to gather and synthesize what little information is available to determine the nature of a given phenomena. In a majority of cases, the capabilities of available detectors serve as the greatest technical limitation to a proposed experiment. Expectedly, detector development has been an area of great continuing research effort in recent decades, especially given the exponential rate at which computer performance has been increasing during this time.

This thesis describes the design, prototyping, and construction of a Multi-Wire Proportional Chamber for use in the Charged Pion Polarizability Experiment at Jefferson Lab's 12 GeV accelerator facility in Newport News, Virginia. Instrumentation electronics will be the primary focus of this document, although mechanical considerations will be mentioned well. Finally, existing data related to the performance of detector electronics will be presented, although performance characterization is still ongoing at this time.

2 Jefferson Lab Accelerator Upgrade

Since 2010, the Thomas Jefferson National Accelerator Facility has been undergoing renovations to nearly double the beam energy to 12 GeV and construct a new experiment hall in addition to the current three. This new hall, named Hall D, will be home to a new detector dedicated to studying the confinement of quarks and gluons in quantum chromodynamics. The new detector, named GlueX, and scheduled to come online in mid-2015, consists of a large electromagnet capable of producing a solenoidal magnetic field. Together with a large array of detectors and other instruments, this strong magnetic field can be used to measure the electric and magnetic polarizabilities of charged hadrons.



Figure 1: A view of JLAB showing the locations of experiment halls A through D. (<http://blogs.umass.edu/miskimen/files/2012/08/jlab.png>)

2.1 12 GeV Accelerator Upgrade

Originally founded as the Continuous Electron Beam Accelerator Facility (CEBAF), the Thomas Jefferson National Accelerator Facility currently houses a 6 GeV electron accelerator. Work is currently underway to increase the beam energy to 12 GeV, which is still only one half of the original 24 GeV design specification.

This upgrade will involve the addition of 10 new cryomodules to the existing configuration. Further, the new cryocavities will be of a 7 cell design as opposed to the 5 cell design currently in place, with the new modules operating at 70 MV each. These modifications will increase the energy gain per pass through the Linac to 1090 MeV for each side for a total gain of 2180 MeV per full pass around the accelerator.



Figure 2: A photograph of one of the the new 7 cell cryomodules. (<https://www.jlab.org/sites/default/files/cavity1.jpg>)

The accelerator is capable of directing the beam for a total of 5 passes yielding a

beam of energy 11 GeV that can be directed to any of the three existing experiment halls. Only experiment hall D (currently under construction) will be capable of receiving the full 12 GeV beam. This is made possible by the construction of another arc which allows the beam to pass through the North Linac one more time, yielding a total beam energy of 11.99 GeV.

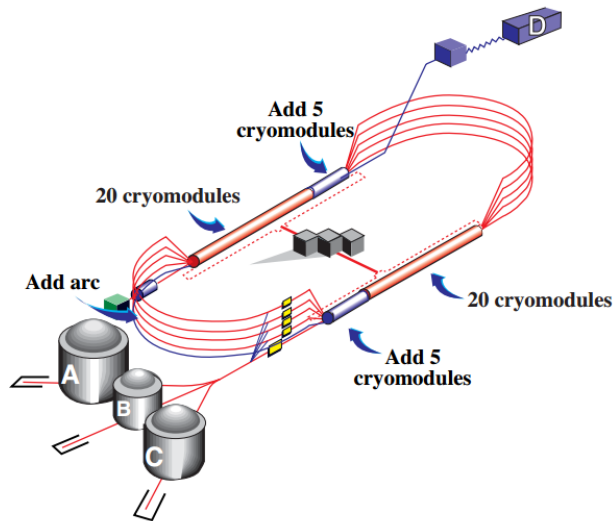


Figure 3: A schematic showing the upgrades being made to the CEBAF accelerator. (<https://accelconf.web.cern.ch/accelconf/p05/PAPERS/TPPP016.PDF>)

(<http://accelconf.web.cern.ch/AccelConf/p03/PAPERS/TPAB085.PDF>) <https://accelconf.web.cern.ch>

2.2 Hall D Addition and the GlueX Detector

The upgrade currently under way will include the construction of a new above-ground experiment hall (Hall D) which is being constructed at the east end of the CEBAF north linac. This new experiment hall is to house the GlueX detector which is currently under construction.

The complete GlueX setup will include diamond crystal resonators with a collimator 75 metres downstream to produce a beam of linearly polarized photons with energies between 8.5 and 9 GeV by coherent Bremsstrahlung emission from 12 GeV electrons. The photon beam will then enter the 2.2 Tesla superconducting coil which houses the barrel calorimeter,

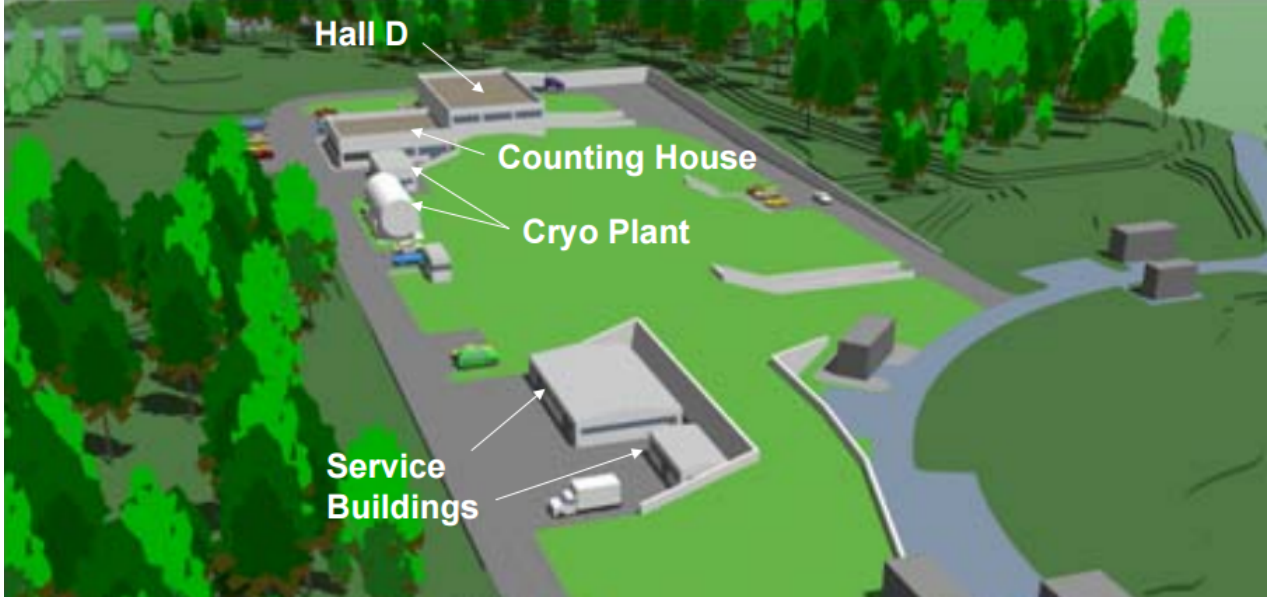


Figure 4: A rendering of Hall D and related support buildings (https://www.jlab.org/exp_prog/PACpage/PAC30/talks/PAC30_v4Elton.pdf)

the central drift chamber, and the forward drift chambers as well as the target. In order to reduce the cost of the project, the solenoid coil to be used in the GlueX detector will be a refurbished version of one previously used in the LASS experiment at SLAC and the MEGA experiment at LANL.

Located immediately downstream of the solenoid assembly will be a scintillating hodoscope for triggering and for time-of-flight (TOF) measurements and a 2800-element lead-glass electromagnetic calorimeter used to scattered photons. To further reduce costs, this calorimeter is being reconfigured from a similar device previously used in the Brookhaven National Laboratory's E852 experiment.

This configuration has been the subject of several Monte Carlo studies for a wide variety of final states to assess the suitability of the detector for carrying out the final analysis. These studies suggest the detector has close to a 4π hermeticity with respect to momentum/energy and position information for charged particles and photons produced from incoming 9 GeV photons. The geometrical acceptance of the detector for final state particles is expected to be above 95% and quite uniform over the detector. (<https://www.jlab.org/12GeV/4>).

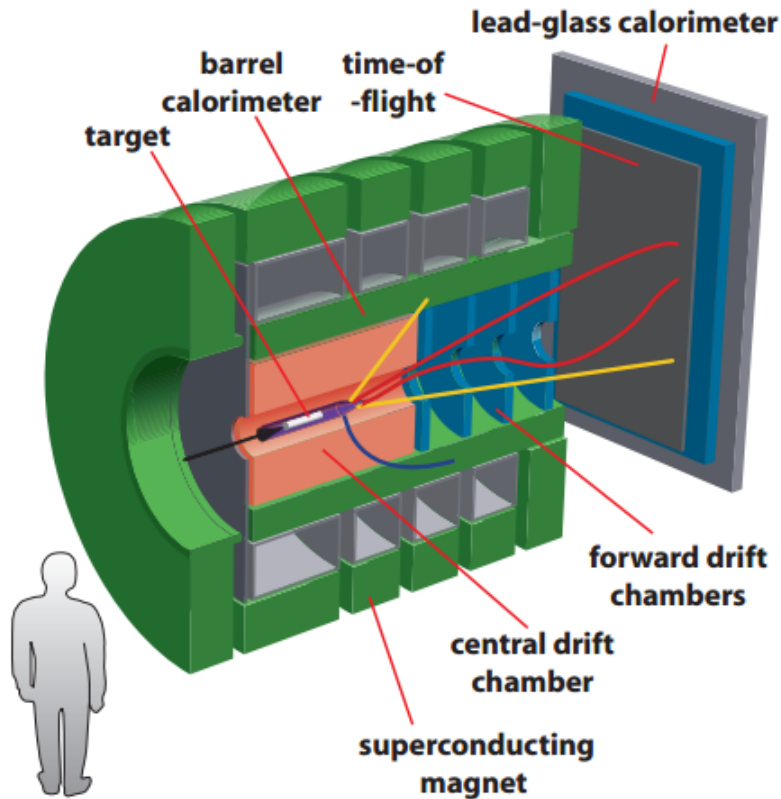


Figure 5: A cutaway view of the GlueX detector apparatus currently under construction in Hall D with a human figure for scale. (http://www.glueX.org/docs/pac36_update.pdf)

2.3 The Charged Pion Polarizability Experiment

One of the first experiments to be performed with the GlueX detector will be to measure the polarizability of charged pions using of the Primakoff reaction. The electric and magnetic polarizabilities of hadrons are best probed in Compton scattering experiments by measuring deviation in the observed scattering cross section from predictions of structureless Dirac particle. Unfortunately, pions don't exist as free particles and as a result, previous experiments utilizing Compton scattering have had to deal with substantial uncertainties in their data. It is believed that by making use of the Primakoff reaction, these uncertainties can be substantially reduced. (R. Miskimen, 2012)

The Primakoff reaction can be treated as the Compton scattering of a pion off of

a virtual photon, within the Coulomb field of a nucleus, and the transfer of a very small amount of momentum to that nucleus. This reaction can be represented as $\gamma\gamma^* \rightarrow \pi^+\pi^-$. (A.V. Guskov, 2010) By measuring the cross-section of this reaction with the GlueX detector, it should be possible to measure the polarizability of the pion with greater certainty than was achieved in previous experiments.

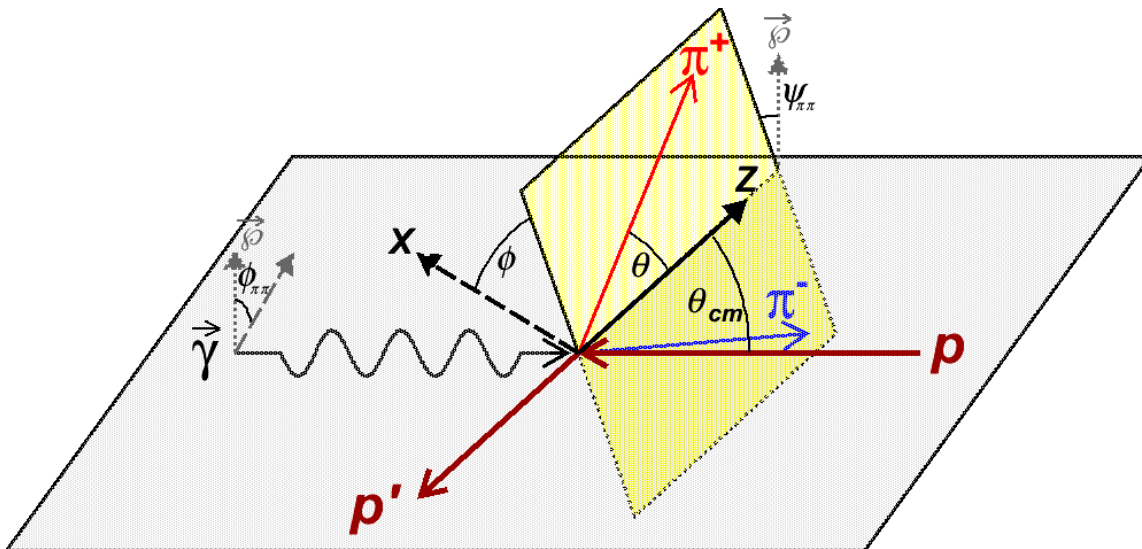


Figure 6: A diagram showing Primakoff Reaction Scattering. (https://halldweb1.jlab.org/wiki/index.php/File:Scattering_angles.png)

Most of the hardware required by the experiment is part of the original specifications for the GlueX detector, however addition detectors must be constructed to enable the positive identification of muons. The required detector assembly will be located several meters downstream of the GlueX detector and will consist of hadronic absorbers (iron sheets several inches thick) with muon detectors sandwiched in between at regular intervals.

A portion of the detector hardware necessary for the Charged Pion Polarizability Experiment is contracted to be designed and constructed at the University of Massachusetts under the guidance of Professor Rory Miskimen. This hardware consists of roughly 10 Multi-Wire Proportional Chambers (MWPCs) which will be situated downstream of the lead-glass calorimeter and will be used to identify muons in the beam line such that they are not confused for pions. Pions and muons have similar masses and identical charge and it is

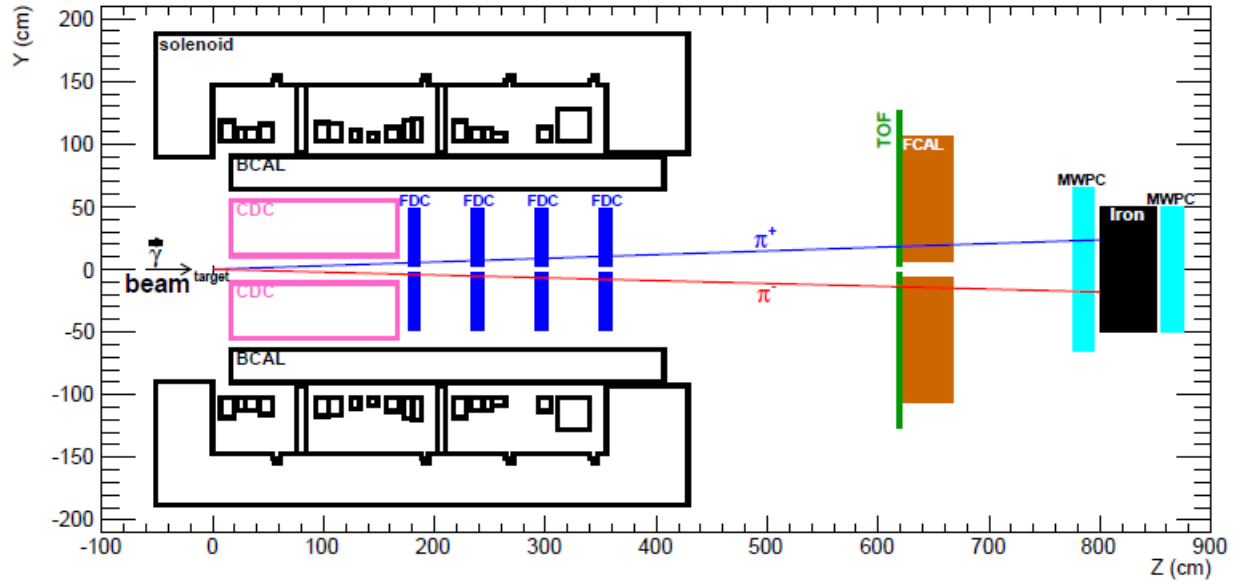


Figure 7: A schematic showing the location of all detector hardware related to the pion polarizability experiment. (PR12-13-008.pdf)

difficult to distinguish the two particle types with the unmodified GlueX setup.

3 Wire Chamber Operating Principles

For nearly 50 years now, the wire chamber has been the work horse of particle physics experiments worldwide. First constructed by Georges Charpak in 1967, wire chambers quickly superseded other methods of particle detection due to the speed and accuracy with which they allow data to be taken. Further, wire chambers continue to remain relevant even as newer solid state detection technologies mature due to the simplicity of their maintenance and operation and their resilience to damage by ionizing radiation.

3.1 Overview of Wire Chambers

In its most general form, a wire chamber consists of a large network of evenly spaced parallel wires mounted to a rectangular frame, each of which acts as a particle detector. These wires are sandwiched between two large conducting planes. A high voltage power

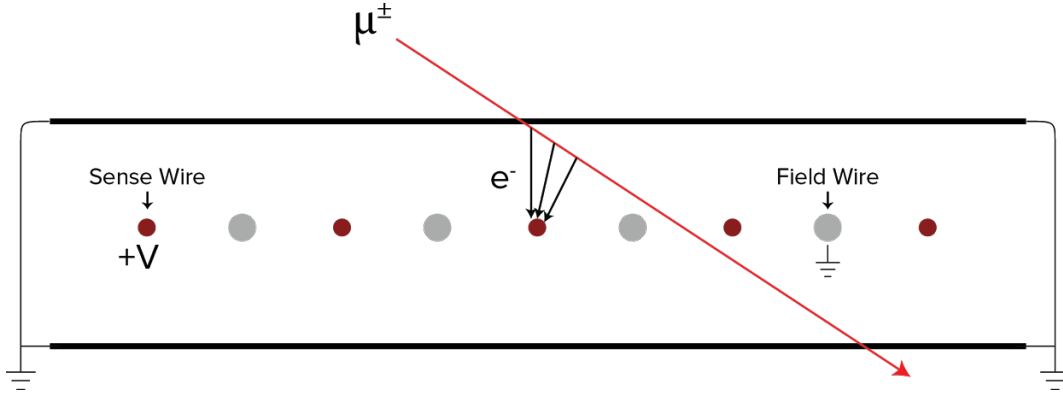


Figure 8: A side view of a Multi-Wire Proportional Chamber (MWPC).

supply is used to create a large potential difference between the wires and the conducting planes, typically of a few kilovolts.

The wire frames, together with the large conductive planes, forms a gas tight pressure vessel. The space inside the detector is filled with a gas of a controlled composition, typically with a slight overpressure relative to the atmosphere. When an energetic particle passes through this gas volume, it ionizes atoms along the path that it took through the detector. Due to the high electric field in the detector, the resulting positively charge atoms drift towards the negatively charged anode and the negatively charged electrons drift towards the positively charged cathode. In the case of the detectors being constructed for the Charged Pion Polarizability experiment, the wires serve as the cathode and the electrons drift towards them.

When these electrons impinge on the wires, it creates a small current proportional to the energy of the ionizing particle. This current is amplified and converted to a voltage signal by a trans-impedance amplifier (TIA) attached to each sense wire. This voltage signal can then be read off by a computerized Analog-to-Digital Converter (ADC), and with sufficient data points, the path and energy of the ionizing particles can be calculated. Chambers which are primarily used to assess path and energy are typically referred to as Multi-Wire Proportional Chambers, while chambers used to also assess drift times are often simply called drift chambers and read out to Time-to-Digital Converters (TDCs).

3.2 MWPC Detector Operating Principles

While the basic operation of an MWPC as described above is fairly straight forwards, as with many things, the devil is in the details. Successful detection of an ionization event, such as a high-energy particle passing through the detector, is dependent on an avalanche effect that increases the number of free electrons impinging on the sense wire.

When an ionizing particle passes through the MWPC, the electromagnetic interactions between the gas atoms and the particle excites and ionizes the gas in what is called an ionization event. The ionization event produces a positively charged atom and a negatively charged free electron. Because it is located in a strong electric field, the electron is acted on by a force in accordance with Coulomb's inverse-square law and accelerates towards the wire.

As the electron gains kinetic energy, it interacts with other gas atoms leading to further ionization events. These events in turn generate more free electrons which themselves are accelerated in the electric field inside the detector until they cause further ionization events. In this way a cascade of thousands of ionization events and subsequently thousands of free electrons are generated for each atom ionized by the original ionizing particle that is being detected. This is known as a Townsend avalanche or a Townsend discharge and the ratio of the final number of electrons produced to the initial number of electrons is known as the gas gain.

The sensitivity and resolution that can be obtained by a detector are highly dependent on the gas gain that a given wire chamber configuration can achieve. If the gas gain is too low, then the detector will be insensitive to low lower energy particles which generate fewer initial ionization events. If the gas gain is too high, then the a single low-level event may overwhelm the detector and make it difficult to distinguish between between different particles or multiple ionization events.

Gas gain is primarily sensitive to the bias voltage of the detector and the composition of the gas being used, although a weaker dependance on operating temperature and

pressure has been noted in literature. (Add citation) For the purposes of this experiment, we anticipate requiring gas gains in the range of $10^4 - 10^5$. This will involve operating the chamber with a gas mixture primarily composed of argon and carbon dioxide with trace amounts of freon, and at a bias potential of roughly 2000 volts, however final operating parameters will be determined experimentally.

4 Detector Design Constraints

The detector being developed is subject to several external design constraints, relating to compatibility with existing facilities and equipment, overall detector performance, and operational safety. Several of these design constraints relate directly to circuit design and PCB layout, while others relate indirectly but must also be taken into account.

4.1 Detector Geometry

Overall detector size and wire plane geometry were largely fixed by the other parameters of the experiment, most importantly, the expected trajectories of scattered particles downstream of the target. Computer simulations performed using Sim-Recon, the GlueX simulation software package, were used to study required detector acceptance and resolution (Citation needed). Based on the results of these simulations, the majority of the particles of interest will be within a radius of 0.75 metres of the beamline center. Thus, in order to realize reasonable acceptance ratios, the decision was made to make the external dimensions of the detectors roughly 2 metres square. This allows the majority of particles to pass through the active area of the detector sufficiently far away from the frame components that boundary effects on the electric field are negligible.

The distance between two adjacent wires, also known as the wire-spacing, is constrained by the desired resolution of the detector. At best, a detector can resolve two simultaneous events only if they occur greater than one wire-spacing length from each other.

In practice, some electrons will usually drift to adjacent sense wires thus decreasing how precisely a given event can be localized, but this effect can be minimized by the addition of grounded field wires between adjacent sense wires. Thus, increasing the resolution of a detector requires that wires be spaced closer together. Unfortunately, as the wires come closer together, the electric field between a sense wire and an adjacent field wire may become strong enough that it leads to arcing. Maintaining this close spacing would require decreasing the bias voltage which would decrease chamber gain. We found a wire-spacing distance of approximately 1 centimetre to be a reasonable compromise between resolution and gain in our detector. Combined with the required active area of approximately 1.5 metres * 1.5 metres, this yielded a design which would feature roughly 150 instrumented sense wire channels.

4.2 HV Isolation

Important design constraints in this project relate specifically to operator safety, ease of maintenance, and the ability to safely place the detector hardware near to or in direct contact with other components of the GlueX detector. The single biggest obstacle to meeting this constraint is the high electrical potential that the MWPCs require to operate properly.

Most existing MWPC designs feature instrumented sense wires held at or near ground potential serving as the anodes with large conductive planes above and below the sense wires as cathodes. The cathodes are held at some large negative potential relative to the sense wires by a current-limiting high voltage (HV) power supply. This arrangement has substantial advantages with regards to the simplicity and ease of design of its circuitry because it allows the amplifiers to be directly coupled to the sense wires and also simplifies PCB design as there are no high voltage signals to be routed on the board. Unfortunately, it also complicates the installation and maintenance of the detector as it will have large exposed areas held at high voltage. Further, the detector would have to be held in place using non-conductive mounting hardware to isolate the detector from the rest of the GlueX detector.

As a result, in the detectors currently under construction, the large metal planes are held at ground potential and the sense wires are held at a substantial positive potential relative to ground. By keeping the aluminum planes at ground, the detector does not have to be electrically isolated from its environment. Further, the detector no longer presents a high voltage safety hazard while biased, which has the potential to make debugging and maintenance of the detector substantially easier.

Biasing the sense wires is achieved using a parallel network of 1 megaohm resistors in series with the sense wires. These resistors are mounted on the PCB that is on the opposite side of the detector from the PCB holding the amplification circuitry and serve to limit the maximum current delivered to the sense wires. Henceforth, this PCB will be referred to as the biasing board or biasing PCB. Because the amplifier circuit cannot handle the high voltages used to bias the detector, the time-varying signal from a passing ionizing particle is decoupled from the time-invariant high voltage bias potential on the sense wire using a 10 nF capacitor with a sufficiently high breakdown voltage. Surface mount ceramic capacitors were chosen for this role because their low profile makes it possible to mount them on the portion of the amplifier PCB which is internal to the detector. In this way, all high voltage traces on the PCBs with the exception of the high voltage connectors are isolated within the controlled environment inside the detector.

4.3 ADC Constraints Differential Output Signaling

The type of Analog to Digital Converter (ADC) to be used with the detectors also imposes certain constraints on the design of the preamplifier electronics, including determining the type of connector to be used and format of the signal output. An ADC is a device which takes a time varying analog signal and discretizes it at predetermine time intervals to produce a series of digital data points. In this way, the complex physically significant information encoded in the analog signal can be fed into a digital computer for ease of analysis.

The JLab 125 MHz Flash ADC module (fADC125) currently under development by

the Jefferson Lab Data Acquisition group, has already been selected for this purpose. The fADC125 is designed to take a 12 bit sample (2^{12} possible values over the supported voltage range), store it along with header information as a 32 bit word, and transmit it 125 million times per second or once every 8 nanoseconds. (citation)

Each fADC125 module consists of a VME card supporting 72 different inputs spread over three different connectors per module, which each connector mating to one preamp board. The connector used in the fADC125 is the 10250-1210pe manufactured by 3M. Each connector has 50 pins organized in two rows of 25 each. 48 pins of the connector compose 24 differential signal pairs carrying output signals, while the remaining 2 pins are used to drive an onboard pulser which can be used to calibrate and test the amplifiers.

Given that the expected number of instrumented sense wires based on the geometry of the detector is approximately 150, and that each ADC module has 72 inputs, it was decided that two ADC modules would be devoted to each detector giving a final count of 144 sense wires per detector.

4.4 On-board Pulser

Due to small variations in the manufacturing process, no two electrical components exhibit the exact same characteristics. As a result, each completed amplifier circuit will produce slightly different responses to the same input. In order to collect accurate data, the amplifiers will have to be calibrated against a known input signal. To do this, a pulser is being incorporated on the amplifier PCB.

The test signal will be generated by the ADC module itself and transmitted to the board as a differential pair carrying a high amplitude square wave. On board circuitry will convert the differential signal to a single ended output which will capacitively couple to the signal traces. In this way, it is possible to achieve uniform coupling without increasing parts count or causing too much cross-talk between different channels .

5 Conceptual Design of Trans-Impedance Amplifiers

The Trans-Impedance Amplifier (TIA) is one of the canonical op-amp circuits taught to every undergraduate electrical engineering student. It finds applications in everything from children's toys to medical instrumentation, and yet despite its pervasiveness, proper TIA design remains challenging.

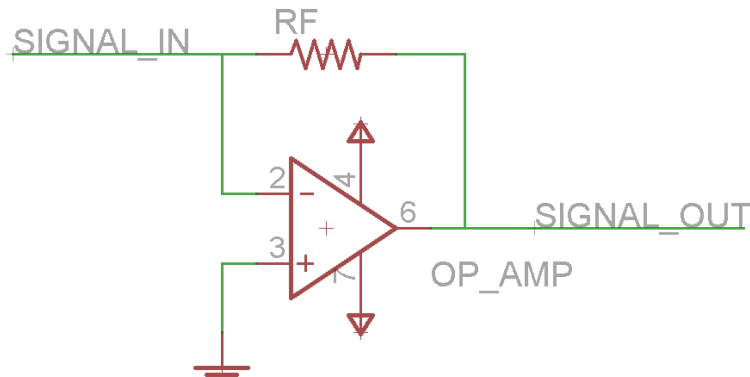


Figure 9: A schematic diagram showing a highly simplified TIA.

In its most basic form, a TIA or current-to-voltage converter, accepts a current signal and produces a voltage signal which is directly proportional to it. The constant of proportionality, called the trans-impedance gain of the amplifier, defines the ratio of output voltage and input current. The amplifier gain is set by the value of the feedback resistor (R_f) used to connect the op-amp output to the inverting input.

$$G = \frac{V_{out}}{I_{in}} = -R_F \quad (1)$$

5.1 Basic TIA Operating Principles

All that is required to understand how the a basic TIA operates is an understanding of the Ohm's law and how op amps function. The op amp, short for operational amplifier, is a type of differential amplifier with a very high open loop differential gain (G typically greater than 100,000), and very high input impedance. A typical op amp will have two inputs (an

inverting input and a non-inverting input) and one output whose potential relative to ground is equal to the difference between the non-inverting input and the inverting input, multiplied by the gain of the amplifier.

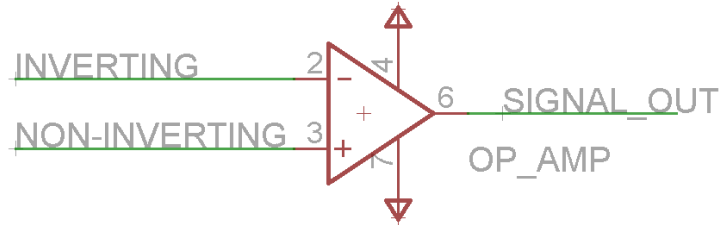


Figure 10: A schematic diagram of a basic op-amp showing the inverting and non-inverting inputs.

$$V_{out} = G * (V_{non-inverting} - V_{inverting}) \quad (2)$$

As a result of this high gain, op amps are almost never used in an open loop configuration and instead rely on negative feedback for proper operation. When this type of feedback is allowed, the op amp will produce a voltage on its output pin which effectively minimizes the difference between the inverting and the non-inverting inputs.

When configured as a trans-impedance amplifier, a resistor is connected between the inverting input and the output of the op amp while the non-inverting input is held at some fixed potential, although usually grounded. When the inverting input to the op amp is left floating (unconnected), both the inverting input and the output of the op amp rest at ground potential and there is no current flowing across the feedback resistor. When a current signal is present on the inverting input, it will be either syncing or sourcing current to or from the node attached to the inverting input of the op amp. Because of its high input impedance, the op amp interprets this as a small potential being asserted on the inverting input.

The op amp responds by generating a voltage signal on the output pin which is proportional to the difference in potential between the two inputs. This causes a current to flow across the feedback resistor which is equal to the magnitude of the current signal

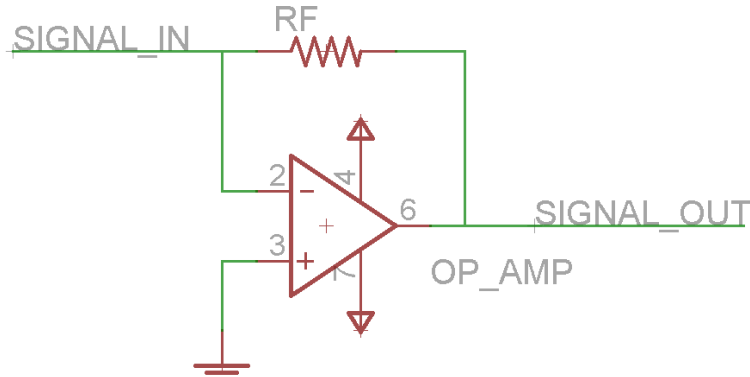


Figure 11: A schematic diagram showing a highly simplified TIA.

being applied to the TIA, but flowing in the opposite direction. As long as the feedback current is equal and opposite to the input current, the output potential of the op amp remain constant. When the input current varies, the op amp will vary its output to re-establish this equilibrium.

5.2 Useful Performance Metrics

TIA performance for a fixed gain is assessed primarily with regard to two different properties, bandwidth and signal noise. Both of these factors drastically affect the overall performance of the amplifier and its ability to faithfully convert a current signal to a voltage signal. Unfortunately, it can difficult to optimize for both of these characteristics at once and a compromise between the two must be found.

Bandwidth relates to the range of frequencies that the TIA can reproduce without resulting in significant signal degradation. A circuit's overall bandwidth is different from the rated bandwidth of any one component, although component choice is the single largest factor in determining a circuit's bandwidth. For example, an op-amp may have a rated bandwidth of 200 Mhz meaning that it will function for signals from 0 hz to 200 Mhz and a transformer that is connected to it may be rated to operate from 10 MHz to 600 Mhz, then the overall cicruit will at best be limited to operating within the range from 10 Mhz to 200

Mhz.

Signal bandwidth can be quantified by feeding a sinusoidal current signal at a fixed amplitude into the amplifier and studying the resulting output signal for signs of signal degradation. The degradation may manifest as either a significant decrease in the amplitude of the signal or, if the output signal is being plotted against the input signal, a substantial phase shift between the two signals.

The second important metric of the performance of a TIA is the magnitude of the electrical noise present in the output signal. Electrical noise is the small random fluctuations which occur in all electrical circuits as a result of electromagnetic interference, thermal noise, and small defects in the electronic components. In practice, it is a fact of modern life and cannot be eliminated, only minimized.

Digital circuits make use of logic levels with a sufficient potential difference that the small variations due to most forms of noise are negligible and do not affect the circuit's operation, but this is not the case for analog circuits. As a result, noise mitigation is a major concern for analog hardware engineers. Some noise and feedback can be eliminated by decoupling the power supply pins on various chips from each other and using ferrite beads to filter out any AC component on the power supply lines. Further noise mitigation can be realized by placing the entire circuit inside a conducting box such that it acts as a Faraday cage and isolates the circuits from external interference.

Noise in an analog circuit is most easily quantified by the signal-to-noise ratio (SNR) which is a comparison of the magnitude of a desired signal to the magnitude of any remaining noise. This can be done using the Fast Fourier Transform function available on most modern digital oscilloscopes. The FFT breaks the input signal down into its component sine functions and graphs the relative magnitudes of each sine function. When the amplifier circuit is given a 5 MHz sine wave as input, the FFT of the output should ideally only show a single peak at 5 MHz. Realistically, there will be many smaller peaks visible as well. Because the FFT measures the amplitude at a given frequency in decibels (dB), the SNR is defined as 10 times

the logarithm of the ratio of signal powers, where the ratio of signal powers is equal to the ratio of the square of signal amplitudes.

$$SNR = 10 * \log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) = 10 * \log_{10}\left(\frac{A_{signal}^2}{A_{noise}^2}\right) \quad (3)$$

5.3 Challenges in TIA Design

While thus far, the design of a transimpedance amplifier may seem rather straight forward, in practice, there is sometimes more witchcraft to it than science. The analyses presented thus far rely on certain ideal assumptions about op amp behavior and the behavior of the rest of the circuit as a whole. For example, we have completely ignored the parasitic capacitances on all traces as well as the capacitance of the sense wire relative to ground. This is a pretty safe assumption to make for most circuits, but it can affect the behavior of high speed circuits such as this one.

A capacitor is formed anywhere that two different circuit elements at different potentials are separated by some finite distance. To that extent, they exist everywhere in a circuit and between every node in a circuit. The capacitance between two circuit nodes is directly proportional to the area of the conductor and the inversely proportional to the distance between the conductors. An exact expression for capacitance can be derived analytically for many simple conductor geometries, although computer software is available to numerically calculate capacitances when this is unfeasible. The most commonly used expression for capacitance is that for a parallel plate capacitor which is shown below where C is capacitance, k is the relative permittivity of the dielectric between the conducting plates, ϵ_0 is the permittivity of free space, and A and d are the parallel plate area and the distance between the plates, respectively.

$$C = k * \epsilon_0 * \frac{A}{d} \quad (4)$$

Fortunately, in most cases, the parasitic capacitance is essentially negligible due to a large separation between circuit elements or relatively low conductor area. In these cases, the circuit will behave fairly ideally and no further design optimization is necessary. When this is not the case, parasitic capacitances may lead to sluggish circuit performance or the seemingly anomalous conduction of AC current between isolated conductors.

Also, we have assumed that our op-amp behaves ideally. The characteristics of the ideal op amp include, but are not limited to:

- Infinite open-loop gain
- Infinite input impedance
- Zero output impedance
- Infinite bandwidth
- Infinite slew rate
- Zero noise

In reality, all op amps deviate from ideal behavior, but this is not a problem for most circuits. For circuits operating at low frequencies and using very clean power supplies, non-infinite bandwidth and slew rate do not affect the operation of the circuit and electrical noise will be sufficiently small compared to the magnitude of the signal that noiseless operation can be approximated. As operating frequency increases, the op amp may no longer be able to respond fast enough to changes in the input signal and it leads to signal degradation. Similarly, when many amplifiers are powered off of one power supply or the power supply is located a significant distance from the amplifier circuit, the circuit may pick up ambient electrical noise or suffer from “ringing” or feedback and crosstalk between adjacent amplifier channels. Similarly, the circuit will be subject to JohnsonNyquist noise or electrical noise generated by the thermal agitation of the charge carriers such as electrons, as well as other

effects arising from small lattice defects in the semiconductor used to make the op amp. All these factor, if left unchecked, may make an amplifier unusable.

Another simplifying assumption in the previous analysis relates to the overall feedback factor and consequentially, the overall gain of the amplifier. Previously, the only feedback element was said to be a resistor, however in practice, some non-negligible feedback capacitance is also required to stabilize the TIA and avoid uncontrolled oscillation. Circuit designers must be extraordinarily careful when determining feedback capacitance (Cf) because if Cf is too low, it will not be successful in suppressing ringing in the circuit and if Cf is too high, it will severely degrade than bandwidth of the circuit. Thus the goal when determining Cf is to find the minimum value which stabilizes the circuit. The required capacitance varies widely and is dependent on the properties of the op amp, the values and configurations of passive components connected to the op amp, and the type of signals the amplifier will be used to amplify, however as a rule of thumb it will usually be in the range of 1 to 20 pF.

To calculate the actual ideal value for Cf, it must first be understood why Cf is necessary. To do this, it is useful to make a plot comparing open-loop gain and feedback factor for an transimpedance amplifier assuming that there is no feedback capacitance. (Maxim stabilize your tia) The single-pole response for the uncompensated circuit can be expressed as

$$A_{OL,j} = \frac{A_{OL}}{1 + j\frac{\omega}{\omega_{PD}}} \quad (5)$$

Where $A_{OL,j}$ is the open loop gain at some frequency ω , A_{OL} is the open loop gain for DC operation, and ω_{PD} is the dominant-pole frequency. Approximating the total input capacitance as the sum of the capacitance of the sense wire and the capacitance of the inverting input, the feedback factor for the entire circuit can be calculated as

$$\beta_j = \frac{X_{C_i}}{Z_f + X_{C_i}} = \frac{1}{1 + j\omega R_F C_i} \quad (6)$$

Where β_j is the feedback factor, R_F is the feedback impedance and C_i is the total input capacitance. Plotting the reciprocal of feedback factor and the open loop gain versus operating frequency yields the plot shown in figure 0000000000000000.

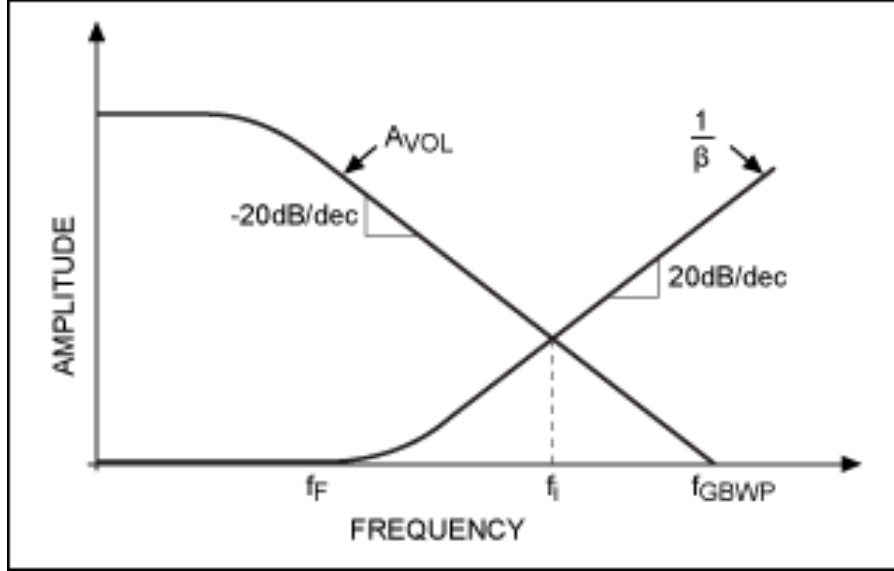


Figure 12: Cite from Maxim application note

According to the Barkhausen stability criterion, the circuit will oscillate if the magnitude of the loop gain is equal to unity, $|A_{OL,j}\beta| = 1$. Thus, the intersection of the curves of $1/\beta_j$ and $A_{OL,j}$ is a critical point for understanding the stability of the circuit. For frequencies that yield $|A_{OL,j}\beta| > 1$, the circuit will exhibit relative stability, while for $|A_{OL,j}\beta| \leq 1$, the circuit will be unstable or exhibit significant phase shift. Thus, the easiest way to ensure stability is to constrain $|A_{OL,j}\beta| > 1$, where $A_{OL,j}\beta$ is the combined transfer function of the op amp and feedback network.

To calculate a value of C_f which satisfies the Barkhausen criterion, the transfer function describing the circuit inclusive of the feedback capacitor must be formulated. If the op amp is assumed to be perfectly ideal, then inverting input is held at virtual ground and the input capacitance has no effect, so the output of the circuit is

$$\frac{V_{out}}{I_{in}} = \frac{-R_F}{1 + j\omega * C_F * R_F} \quad (7)$$

and the transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{-1}{1 + j\omega * C_F * R_F} \quad (8)$$

This is consistent with an intuitive understanding of how the circuit operates at either very high or very low frequency. For low frequencies, where $s \ll 1$, the circuit simplifies to the basic transimpedance amplifier that was previously described. For high frequencies, or where $s \gg 1$, the complex impedance in the denominator of equation 0000000000 dominates. Furthermore, this equation yields a pole at $f = \frac{1}{2\pi R_F C_F}$ which can be seen in figure 00000000000, labelled as .

Unfortunately, the op amp does not behave this ideally and as a result, the input capacitance must be taken into account. By treating the total input capacitance as some complex impedance to ground, the feedback factor can be calculated by taking the ratio of impedances:

$$\beta_j = \frac{V_{in}}{V_{out}} = \frac{\frac{1}{j\omega C_{in}}}{\frac{1}{j\omega C_{in}} + \frac{R_F}{1 + j\omega C_F R_F}} \quad (9)$$

which simplifies to:

$$\beta_j = \frac{1 + j\omega C_F R_F}{1 + j\omega (C_{in} + C_F) R_F} \quad (10)$$

This equation yields a pole of $f_i = \frac{1}{2\pi R_f C_F}$ and a zero of $f_F = \frac{1}{2\pi R_F (C_f + C_{in})}$. Both of these points are seen in figure 00000000000.

The equation for A in this case is the same as the gain bandwidth product:

$$A_{OL,j} = \frac{\omega_{GBW}}{\omega} = \frac{f_{GBW}}{f} \quad (11)$$

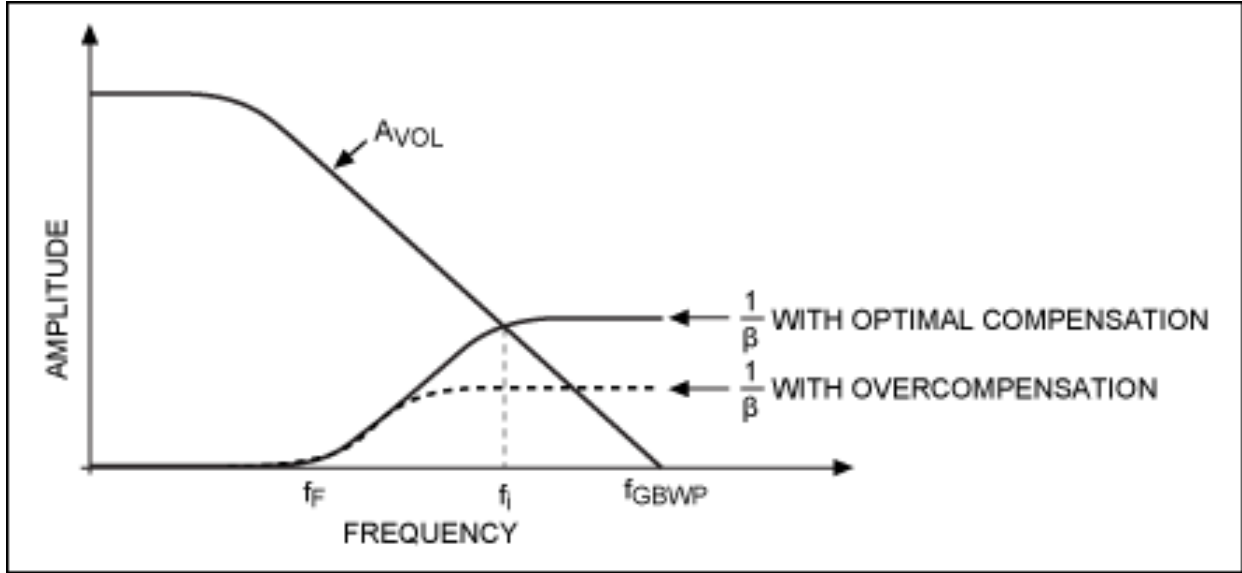


Figure 13: Cite from Maxim application note

Thus:

$$A_{OL,j}\beta_j = 1 = \frac{f_{GBW}}{f} * \frac{1 + j\omega C_F R_F}{1 + j\omega(C_{in} + C_F)R_F} \quad (12)$$

Because $A_{OL,j}$ intersects $1/F$ at its pole:

$$\omega = \frac{1}{C_F R_F} f = \frac{1}{2\pi C_F R_F} \quad (13)$$

and

$$f = \frac{1}{2\pi C_F R_F} \quad (14)$$

Using these two relations to solve equation 000000000 yields:

$$8\pi^2 f_{GBW}^2 C_F^2 R_F^2 = 1 + \left(\frac{C_F + C_{in}}{C_F}\right)^2 \quad (15)$$

This equation does not lend itself to an easy analytical solution for C_F and if an exact solution is necessary, a numerical method should be used. A solution can be approximated

using the assumption that $C_{in} \gg C_F$. In this case, it is possible to approximate the ideal value of the feedback capacitance as:

$$C_F = \sqrt{\frac{C_{in}}{2\sqrt{2}\pi f_{GBW} R_F}} \quad (16)$$

In the case of the amplifier being designed for this project, equation 000000 yields a feedback capacitance of 0.4 pF for an op amp with $f_{GBW} = 1.6 \text{ GHz}$, $R_F = 10 \text{ kilohms}$, and $C_{in} = 22 \text{ pF}$.

A final consideration that needs to be kept in mind when designing a TIA is the input bias current of the op amp. This parameter directly determines the sensitivity of the amplifier and sets the threshold below which a signal is undetectable. The input bias current of an op amp specifies how much current actually flows into or out of the inputs of an op amp. Ideally, no current flows into the input terminals of an op amp. This is a consequence of approximating the input impedance of an ideal op amp to be infinite, but in practice an op amp has some finite, though very large input impedance. As a result, some small amount of current will flow into or out of the op amp during operation. This small current is negligible in most applications, but when the signal being measured is only a few hundreds of nano-amperes, the bias current may overwhelm the signal and lead to substantial uncertainty in the measured value of the current signal.

5.4 Challenges in PCB Layout

Proper board layout can be as important as good schematic design, especially in high performance applications. In addition to obvious design constraints related to the size and shape of the board and the number of amplifier channels that it must contain, there are other design considerations which relate to how ideally the circuits described in the schematic can be implemented.

It is impossible to design an ideal board, and as a result, compromise must be made

with regards to the electrical properties of a PCB. A well optimized board design seeks to minimize parasitic capacitance between adjacent conductors while also avoiding sharp angles in signal traces and eliminating major ground loops. Parasitic capacitance can, as previously mentioned, lead to slowed circuit performance or a non-infinite complex impedance between two different conductors. It can be minimized by either decreasing the area of adjacent traces or increasing the distance between them.

Ground loops are a completely different phenomena that occur when a full circuit (the path that current will flow along) traces out some large area through which an electromagnetic flux may pass. The circuit's sensitivity to stray magnetic fields is proportional to the area enclosed by this loop in accord with Faraday's Law and therefore, minimizing this area is of great concern. When a differential signals are being used, the two matching traces forming the differential pair are usually routed in parallel with a minimum distance between them. For most circuit boards which use single ended signaling, the return path of any circuit is ground, therefore it makes sense to create a large grounded area of conductor directly under the circuit traces, known as a ground plane.

6 Electronics Prototyping

Regardless of how complete a mathematical analysis is, it will fail to perfectly describe the behavior of a circuit once it is implemented in hardware. Therefore, prior to large scale manufacturing, all electronic circuitry must be prototyped and tested to determine if it meets the specified performance goals. To this end, dedicated tools, such as breadboards, are available to assist in prototyping with larger Dual Inline Package (DIP) components. Unfortunately, many high performance components are not available in breadboard friendly packages. Instead, the manufacturers of these components will often sell an evaluation board which contains the component of interest as well as handful of supporting components. During the course of this project, several evaluation boards were considered, but found to

be unsuitable due to difficulties associated with connecting the board to the detector.

Instead of using evaluation boards, during this project, prototyping was done by designing the prototype board in Eagle CAD, manufacturing the board in low quantities, and assembling the boards by hand. In this way, the cost associated with a prototyping a design iteration could usually be kept under \$100.00. Other advantages associated with this method include mechanical robustness due to all components being on one board, noise reduction by the elimination of potential ground loops, and ease of scaling to a final design.

6.1 THS4631

The first op amp seriously considered for this project was Texas Instrument's THS4631. The THS4631 features a Gain Bandwidth Product (GBP) of 210 MHz, a rated slew rate of 1000 V/ μ s, and an input bias current of only 100 pA. These characteristics would seem to make it ideal for the application at hand. Unfortunately, the high input capacitance of the circuit degrades the effective transimpedance bandwidth of the amplifier, leading to lag and overshoots in the output signal. These properties can be seen in figure 000000000000.

6.2 OPA657

Once it became clear that the THS4631 had insufficient bandwidth for this application, development efforts shifted to focus around a faster op amp, the OPA657, also made by Texas Instruments. The OPA657 has a slew rate of only 700 V/ μ s, but its rated GBP is 1.6 GHz and the input bias current is only 2 pA. Unfortunately, this improved performance comes at higher financial cost with the acquisition price per op amp being nearly twice that of the THS4631.

A board was constructed to test the OPA657 as configured for a trans-impedance gain of 10 kilohms. This circuit was found to give satisfactory performance with a maximum trans-impedance bandwidth of 000000000000 as determined experimentally. This high bandwidth resulted in an output signal with minimal phase shift or distortion relative to the input

signal as can be seen in figure 0000000000000000. Further, the circuit was not found to produce “ringing” or power rail feedback oscillations, and was found have a very high signal to noise ratio of approximately 000000000000. As a result of this performance, the OPA657 was selected for use in the design of the MWPC preamplifiers.

6.3 Other Options Considered

In addition to the two op amps mentioned specifically above, several other were evaluated and found not to be suitable for various reasons. Early in the project, several DIP op amps were tested, however they could not produce the necessary bandwidth and produced very noisy output signals. Two monolithic surface-mount transimpedance amplifiers were also tested. The AD8015 is a monolithic transimpedance amplifier with a rated bandwidth of 240 MHz and differential output. It was designed for use attached to photodiode as used high speed fiberoptic transceivers where it would only be work with digital signals with data rates up to 155 Mbps. Unfortunately, when tested, it proved to be insufficiently sensitive to the low current signals produced by the detector. The other monolithic transimpedance amplifier that was considered is the OPA857 by Texas Instruments. The OPA857 is designed to handle analog signals and has a rated bandwidth of 130 MHz and differential output, just like the AD8015. When tested on a manufacturer supplied evaluation board, the transimpedance gain of the OPA857 proved difficult to control and the monolithic design made fine tuning the circuit impossible. As a result, the OPA857 was deemed unsuitable for this project.

6.4 Adding Differential Output

Because the fADC125 is designed to accept differential input and the OPA657 produces a single-ended output, a method had to be devised to convert between the two. At least initially, the addition of a amplifier stage connected to the output of the OPA657 was considered. Such an amplifier would have to be a constructed from dedicated differential op

amp or perhaps a monolithic single-end-to-differential converter such as the LTC1992 from Linear Technologies. While feasible, this concept was ruled out due to concerns that the second amplifier might lead to feedback with the OPA657 through the shared ground rail.

Instead, a balun was used to convert the amplifier output from single-ended to differential. A balun is a particular type of transformer which has 2 connections on one side and 3 connections on the other. A transformer is a circuit element, typically composed of two coils wrapped around a shared ferromagnetic core, which couples two circuits together inductively. When a time-varying current flows in one side of a transformer, it will induce a current of equal magnitude in the other side. If the two coils are of different impedances, then the transformer may be used to step up or step down a voltage. In the case of a balun, it converts between a balanced signal (differential) and an unbalanced signal (single ended), hence the name balun for a balanced to unbalanced transformer.

Several models of balun were evaluated for use in this project, but two showed real promise: The ADT1-1WT+ from Mini-Circuits and the MABAES0060 from MACOM. These transformers were tested over several frequencies to assess to what extent an output signal was attenuated or distorted due to phase shift. The MABAES0060 was selected over the ADT1-1WT+ because although neither transformer produced a significant amount of lag or phase shift, the ADT1-1WT+ attenuated the output signal to an unacceptable extent.

6.5 Adding an Onboard Pulser

The fADC125 has an onboard signal generator which is to be used to test and calibrate each amplifier channel. The signal generator creates a differential pulse which then must be converted to a single-ended pulse on the amplifier board. Initially, an op amp circuit was considered in this role, but due to concerns about feedback and noise, a transformer was used instead.

Coupling the single-ended output produced by the transformer to each and every sense wire also proved tricky. The nature of the coupling has to be such that signal generator

is able to affect the sense channels, but that individual sense channels are not able to affect each other. This is made slightly easier by the fact that the magnitude of the signal produced by the signal generator is several times larger than that produced by detector, but signal isolation is still a significant concern. Diodes were briefly considered for use in coupling the transformed pulse signal, but a capacitive coupling was ultimately favored. Instead of implementing of using discrete capacitors, this coupling was achieved by forming a low value parallel plate capacitor using traces on each side of the PCB as plates and the 1.6 mm thick FR4 PCB substrate as a dielectric. This yields a capacitance on the order of 1 pf.

7 Planned Final Design

Once several generations of a scaled-down detector have been constructed and tested, and the major technical challenges have been resolved, the amplifier design must be scaled up to fit the final detector. This process was made especially easy by the decision to prototype on actual PCBs instead of utilizing development boards or breadboards. As a result, the scale up process largely consisted of copying a single amplifier channel layout off of the final prototype board and placing it down multiple times in parallel. The only design considerations that remain at this stage relate to how high voltage will be supplied to the biasing boards on one side of the detector and how instrument supply power will be provided to the board holding the amplifier circuits.

7.1 Circuit Schematic

The final preamplifier circuit is based on the OPA657nb op amp manufactured by Texas Instruments. The OPA657nb is configured as a conventional transimpedance amplifier with a feedback resistance of 10 kilohms and a feedback capacitance of 1 pF. The inverting input of the op amp is connected to the DC blocking capacitor by a 100 ohm resistor and the DC blocking capacitor connects to the sense wire within the detector. Also connected to the

inverting input are two 1N4148 fast signal diodes arranged in an antiparallel configuration. These diodes serve to “clamp” the voltage on the inverting input to within ± 0.7 V. of ground, in effect partially protecting the op amp in the events of arcing or some form of power surge. Attached to the junction between the DC blocking capacitor and the 100 ohm resistor to the op amp’s input pin, a 1 megaohm resistor is connected to ground. This resistor serves to slowly drain any residual charge left in the capacitors after supply power to the board is shut off. The capacitive coupling between the pulser circuit and the sense traces is also located just after the DC blocking capacitor, but before the 100 ohm resistor.

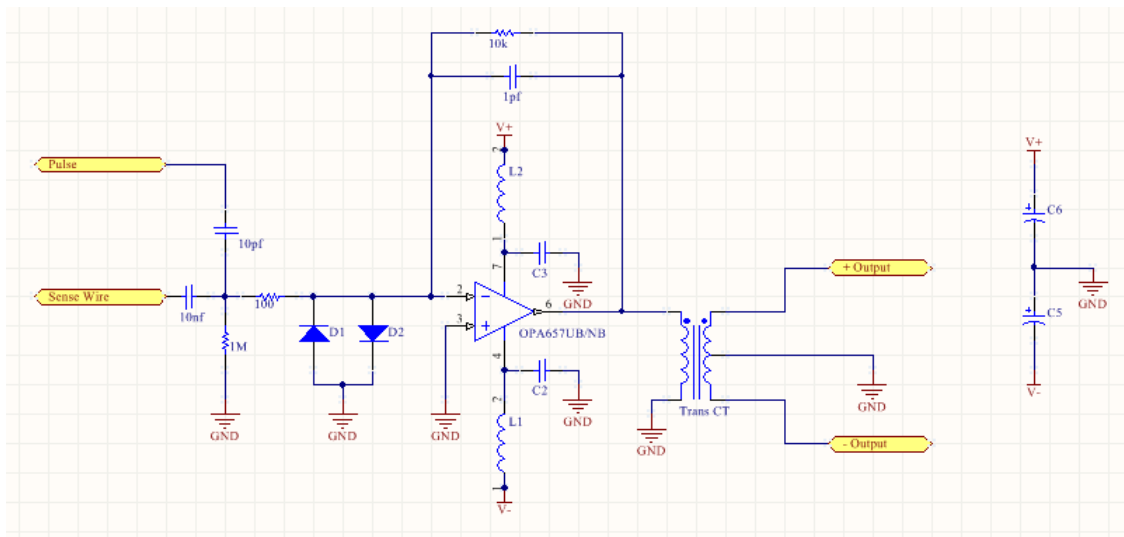


Figure 14: A schematic diagram of the finalized circuit schematic.

The output pin of the op amp feeds into one end of the primary coil on the unbalanced side of the transformer with the other side being connected to ground. On the balanced side of the transformer, the center tap on of the secondary coil is connected to ground such that it will produce positive and negative signals of equal magnitude when a current runs through the primary coil.

The design of the circuitry used to supply power to the op amp is of paramount importance to the performance of the amplifier. The power supply must be able to compensate for small variation in the quality of the power being supplied to the board while preventing cross talk between separate channels through the power supply rails. This is partially

achieved through the use of decoupling capacitors to ground located in close proximity to the op amp's power supply pins. These decoupling capacitors serve to short any high frequency components on the power pins to ground, thus preventing them from affecting the output of the circuit. Ferrites also help to isolate the op amp from variations in the power supply. A ferrite can be thought of as a transformer which has a some fixed resistance permanently attached to its secondary coil. As a result, it will dissipate the energy of any time-varying signal, but allow DC signals to pass. Due to this property, it is often used in the power supplies of high precision instruments where high frequency oscillations on the power rails will negatively affect the performance of a circuit. Finally, large value electrolytic capacitors are placed between the power rails and ground. These serve as a reservoir of charge and in the event that there is a momentary interruption in the external power supply connected to the board.

7.2 Printed Circuit Boards

The dimensions of the final circuit board design are roughly 9.6 inches wide by 7.5 inches deep. This width of the board was fixed by a combination of the wire spacing of the detector and the number of differential pairs per connector. The inter-wire spacing is 0.4 inches, and there are 24 differential pairs per connector, therefore 24 channels per board, hence each board is 9.6 inches wide. The remaining dimensions of the board are not explicitly constrained by the detector geometry.

The board was designed such that all of the components and most of the circuit traces that make up the preamplifier circuit are on the top side of the board. This greatly simplifies the assembly process as only one side of the board needs to be reflowed as opposed to both sides of the board. The only traces located on the bottom are the power rails, a large copper region forming one half of the capacitively coupled pulser circuit, and connections used to hold the field wires at ground potential.

The only unresolved issue with regards to PCB development is how to supply power

to the boards. Both the HV biasing boards and the preamplifier boards are designed to be chained together using soldered-on wires and consequently do not have on-board power connections. The planned solution is to create small PCBs which are placed on either end of a row of biasing or preamplifier PCBs. These smaller boards would have the required power connector on them as well as several un-instrumented wires which will help ensure that the instrumented wires are not subject to any unusual boundary conditions in the electric fields near the edge of the detector. While this solution should definitely be feasible, it is as of yet untested.

8 Conclusions

Despite all the progress that has been made, this project as it stands is incomplete. Instead, it remains an active, living endeavor which will continue beyond my time here at UMass. The majority of the design work has already been completed, however a fair amount of work relating to the final integration of the amplifier electronics into the detector and the construction of the full set of detectors remain.

8.1 Synopsis of Work Completed

Since the beginning of this project, great strides have been made towards achieving the final objective of constructing 10 full-scale MWPC particle detectors. Starting from an incomplete set of specifications, a basic amplifier circuit was designed. From this circuit, a prototype PCB was laid-out, manufactured and subsequently installed in a prototype detector. The detector was tested under a variety of conditions and its performance was measured quantitatively. Based on this data, changes were then made to either the amplifier electronics or the mechanical design of the detector to optimize certain parameters and a new prototype was constructed. This process was repeated several times yielding nearly a half-dozen prototypes. This effort has yielded a highly-refined amplifier design which meets

or exceeds all of the required specifications. Further, all design variables relating to the preamplifiers are now specified and all major design work is now complete.

8.2 Current Status and Remaining Work

What work remains on this project primarily relates to the integration of the amplifier boards into the full-scale detectors and manufacturing. Several prototype-scale detectors have been constructed with full sets of preamplifier electronics, but as of yet, a full size detector has not been constructed, although work is currently under way to do so. Scaling up from the prototype detector to the full-size detector should be fairly easy due to the modular design of the amplifier boards, however it will require the creation of additional PCBs to hold the power supply connectors. There is also a slight possibility that when that 144 amplifier circuits are connected together over shared power rails, it will produce some kind of feedback interference or crosstalk that was not seen in testing with 10 amplifier channels, but this is unlikely.

The other major portion of this project which remains is manufacturing. Once the design has been tested at full-scale, 10 identical full-scale detectors need to be constructed. This will involve ordering hundreds of assembled PCBs, thousands of pounds of custom-manufactured aluminum panels, and nearly two miles each of sense and field wire. This phase is further complicated by the fact that detector assembly must occur in a clean room, and the clean room to be used is located on the third floor of a high-rise office building. Once assembled, each detector must then be crated and shipped to Jefferson lab for final installation. Each of these steps poses a unique logistical challenge which has yet to be solved.

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